Nonlinear Embedding Model for the Accelerated Design of PAs with the ASM-HEMT model

Patrick Roblin*, Miles Lindquist*, Nicholas Miller+ and Marek Mierzwinski^

*The Ohio State University, +AFRL, ^Keysight

http://www2.ece.ohio-state.edu/~roblin/
RF Power Amplifiers

- **Technology**
  - LDMOS
  - GaAs
  - Si Bipolar
  - GaN
  - Others ...

- **Device Models**
  - Basestation
  - Com. Satellite PAs
  - Power → weight → cost

- **PA Design**
  - PA Synthesis
  - Class of PA
  - Harmonic control
  - Matching solutions
  - Package integration
  - Others ...

- **Architecture**
  - Linearization
  - Doherty
  - Envelope Tracking
  - Switch Mode
  - Chireix
  - Others ...

- **Basestation Power Usage**
  - 60% PAs
  - 12% Supplies
  - 18% air-conditioning
  - 10% DSP
Designing PAs By Embedding Waveform Engineering at Package Reference Planes

NEW PARADIGM:
Waveform Engineering at Current Source Ref. Planes

Waveform Engineering at Package Reference Planes

• Single-transistor PA: Class B example for 6 loads

Nonlinear Embedding Model

Nonlinear Charges/Manifold / Package Reference Planes

Harmonic Termination

2-Port

& Matching Network

2-Port

& Matching Network

Parasitics

$\Gamma_S(n\omega)$

$\Gamma_L(n\omega)$

$\Gamma_L.\omega$

$\Gamma_L.2\omega$

$\Gamma_L.3\omega$

$\Gamma_{\text{out}}$ increase
More CATCHING Less FISHING

Embedding PA Design

One single cast

Billions of casts
With multi-harmonic source and load pulling
Nonlinear Embedding & De-embedding

Embedding/De-embedding:
- Circuit based (harmonic balance)
- Model based (no measurements)
- Can include high/low frequency dispersions (self-heating, trap, parasitic BJT)

Embedding model is like ABCD-parameters but nonlinear and in the time domain
Quality of Model via De-Embedding to CRF

**De-embedded internal harmonic loads**

**De-embedded load-lines**

Compare intrinsic data from de-embedding model and model

\[ \text{Intrinsic Load-line Data} \]

- \( V_{GS}, V_{DS} \)
- \( i_G, i_D \)

**Intrinsic Class B**

**MODEL**

**De-Embedding MODEL**

\[ \text{NVNA Measured Data} \]

3 % (foundry) versus 9 % (extracted)
CW and Modulated Meas. with NVNA

Harmonics

VSNA:
- VNA (linear)
- NVNA (large-signal RF)
- VSA (5 channels, PAE)
- DPD dual-input PA

Waveforms

DPD

500 MHz 64 QAM Constellation

5 Channel VSA

0.48 % EVM
Types of Embedding Model:
• Symbolically defined model: Circuit
• Equation based: Verilog-A (easiest to implement)

Embedding Model Developed at OSU:
• Angelov: Circuit & Verilog-A (Keysight)
• OSU Artificial Neural Network model: Circuit
• HBT: Verilog-A (Broadcom)
• ASM-HEMT: Verilog-A

Recent Users & Collabortors:
Mitsubishi, Japan
IIT Roorkee, India
U. Aveiro, Portugal
U. Colorado, Boulder, CO
Modelithics, FL
Keysight Technologies, Inc., CA
CICESE, Mexico
First design intrinsic PA with IV:

\[ i_D = i_{Di} + \frac{dQ_D(v_{GSi}, v_{DSi})}{dt} \]
\[ v_{DS} = v_{DSi} + i_D R_D \]
\[ v_{GS} = v_{GSi} \]

Next move from intrinsic to extrinsic reference planes: Embedding

Deembedding moves from extrinsic to intrinsic Ref. Planes

\[ v_{GSi} = v_{GS} \]
\[ v_{DSi} = v_{DS} - i_D R_D \]
\[ i_{Di} = i_D - \frac{dQ_D(v_{GSi}, v_{DSi})}{dt} \]
Circuit Example: Angelov Model

Angelov Device Model

Testbed Package Extrinsic

Current Source

Angelov Embedding Device Model (here up to extrinsic plane)

- No convergence problem (layered)
- Thermal dispersion included
- Exact

(Jang, MTT 2014)
Verilog-A Example: ASM-HEMT

\[
\begin{align*}
\text{I_{de, OSU}} &= \text{Id_{1, OSU}} - \frac{d dt(q_{bdov}) - (d dt(q_{dov}) + d dt(q_{fr})) + (d dt(q_{dsov}) - d dt(q_{fr3}) - d dt(Q_{dep}))}{d t} \\
\text{I_{ge, OSU}} &= \text{I_{gi, OSU2}} - \frac{d dt(q_{bdov}) + (d dt(q_{dov}) + d dt(q_{fr})) + (d dt(q_{sov}) + d dt(cfgd*V_{gse}))}{d t} \\
\text{I_{se, OSU}} &= \text{I_{de, OSU}} + \text{I_{ge, OSU}}
\end{align*}
\]
Linear Manifold Implemented as 6-port ABCD Box

\[
\begin{align*}
V_{g}\cdot V_{d}\cdot V_{s} &= A_{g} \cdot A_{d} \cdot A_{s} + B_{g} \cdot B_{d} \cdot B_{s} \\
&= C_{g} \cdot C_{d} \cdot C_{s} + D_{g} \cdot D_{d} \cdot D_{s}
\end{align*}
\]
Nonlinear Embedding: Class B Example

Or How to Synthesize a Textbook PA Mode

**Input:**
Select desired intrinsic load line

**Output:**
Required external waveforms

With an *Embedding Device Model* a single harmonic balance simulation replaces millions of loadpull impedance searches

*(Jang, MTT 2014)*
Nonlinear Embedding: Class B

\[ Z_L(n\omega) = -\frac{V_{DS}(n\omega)}{I_D(n\omega)} \]

\[ Z_S(n\omega) = -\frac{V_{GS}(n\omega)}{I_G(n\omega)}, \quad n > 2 \]

\[ Z_S(\omega) = \text{conj}\left[\frac{V_{GS}(\omega)}{I_G(\omega)}\right] \]

(Raffo et al, 2009)

Some \( Z_S \) & \( Z_L \) are outside the Smith Chart

Quasi-Textbook Case

(Jang, MTT 2014)
Class F Example with 3 Harmonics

\( v_{DS}(t) = V_{DD} + V_{DS,1} \cos(\omega t) + V_{DS,3} \cos(3\omega t) \)

Shorted @ 2\(^{nd}\) harmonic: \( V_{DS,2} = 0 \)

Open @ 3\(^{rd}\) harmonic: \( I_{D,3} = 0 \)

\( V_{DS,3} = \frac{1}{6} V_{DS,1} \)

Drain Efficiency:

\[ \eta = \frac{P_{RF,1}}{P_{DC}} = 1 - \frac{P_{diss}}{P_{DC}} - \left( \frac{P_{RF,2}}{P_{DC}} + \frac{P_{RF,3}}{P_{DC}} + \ldots \right) \]

with: \( P_{RF,n} = \text{Re}[V_{DS,n} I_n^*]/2 \) and: \( P_{DC} = V_{DD} I_D \)

Orthogonal waveforms

Ideal Class F
- Rectangular voltage: \( v_{DS}(t) \)
- Half-way rectified sinusoidal drain current: \( i_D(t) \)
Experimental Verification of Class F using Embedding

- Apply Class F at the current source reference planes
- After embedding to the Package Ref. Planes, the predicted 3rd harmonic termination is in full agreement with the experimental 3rd harmonic loadpull measurements at the Package Ref. Planes versus Prediction
Class F Simulation with ASM-HEMT

Model and Embedding Models Fully Agree

Nick Miller, AFRL

<table>
<thead>
<tr>
<th>PDC</th>
<th>PRF</th>
<th>eta_D</th>
<th>PAE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.511</td>
<td>1.997</td>
<td>79.534</td>
<td>79.534</td>
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</tbody>
</table>
### CLASS J PA Design Experimental Results

#### Using embedding device model

![Diagram showing output matching and embedded model](image)

**K. Rawat’s Group**
**IIT Roorkee**

<table>
<thead>
<tr>
<th>Ref</th>
<th>PA Type</th>
<th>BANDWIDTH (GHz), (%)</th>
<th>DE (%)</th>
<th>Power (W)</th>
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</thead>
<tbody>
<tr>
<td>[7]</td>
<td>Class-J</td>
<td>1.5-2.5 (50)</td>
<td>60-70</td>
<td>39.5-40.5</td>
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<tr>
<td>[9]</td>
<td>Class-J</td>
<td>2.3-2.7 (15)</td>
<td>&gt;60</td>
<td>40-40.7</td>
</tr>
<tr>
<td>[10]</td>
<td>Class-J</td>
<td>1.6-2.2 (32)</td>
<td>55-68</td>
<td>40-41</td>
</tr>
<tr>
<td>This Work</td>
<td>Class-B/J</td>
<td>1.3-2.4 (59)</td>
<td>63-72</td>
<td>40.1-41.2</td>
</tr>
</tbody>
</table>

This Work

![Photograph of K. Rawat](image)
Designing Multi-Transistor PAs by Embedding

- Two-way PA (Doherty or Chireix)

Testbook DPA theory applies at the CRF
W. H. Doherty

- **15W, 9.54 dB back-off asymmetric Doherty**
  - Using 2 same size 15W GaN device (CGH27015F)
  - Two separate biases, reduced main drain bias

**Intrinsic IV model**

- 15W, 9.54 dB back-off asymmetric Doherty
  - Using 2 same size 15W GaN device (CGH27015F)
  - Two separate biases, reduced main drain bias

**Doherty PA Design at CRF**

- **Main PA**
  - Class F

- **Auxiliary PA**
  - Class C

**Diagram**

- Intrinsic IV model
- Main and Auxiliary PA configurations
- Graphs showing vDS (V) vs. Pin.norm for Main and Auxiliary PAs

**Haedong Jang**

- Doherty PA Design at CRF

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Projected Loads at Package Reference Plane

Projection from *Embedding Device Model*

Main PA

Auxiliary PA

Class F

Class C

Optimal harmonic terminations with slight negative resistance
Verification with LSNA-NVNA

- CW measurements with an LSNA at 2 GHz
- 52% average efficiency for 10 MHz LTE

H. Jang, MTT 2104

Designed, Fabricated and Tested in 3 Weeks
GUI for Automatic Design of Doherty PA

Chenyu Liang

Demoed at RWW in 2019

Doherty PA Designed by Embedding in 24 sec on a Laptop
Doherty-Chireix (Outphasing) Continuum Theory

\[ K_{\text{va}} = \frac{|V_{ap}|}{|V_{ab}|}; K_{\text{ia}} = \frac{|I_{ap}|}{|I_{ab}|} \]

PAs “Load-pulling” each other

Main 1

\[ I_m \]

\[ V_m \]

\[ Z_1 = R_{mp} \]

\[ Z_2 = R_{ap} \]

\[ R_L = \frac{R_{mp}}{n + 1} \]

\[ Z_1, \theta_1 \]

\[ Z_2, \theta_2 \]

\[ 2 \rightarrow 1 \]

Main 2/Aux.

\[ V_a \]

\[ I_a \]

2-Port Network

\[ |V_{ap}| \text{ peak} \]

\[ |V_{ab}| \text{ backoff} \]

Normalized Peak Power

[Diagram of 3D plot showing normalized peak power with Doherty and Chireix points indicated]

[Diagram of graph showing ratio \( K_{\text{va}} \) with peaks and backoffs indicated]
Broadband PA Design with Embedding

1.4 to 2.5 GHz

On-Chip Realization

3.5 to 7 GHz

Dominique Mikrut
Advantages of PA Design using Embedding

• The *nonlinear embedding model* eliminates replaces time-consuming *multi-harmonic loadpull* and *source* simulations by a *single* simulation
• Automatic Design of Narrowband PAs
• Facilitates broadband PA design
• Verilog-A Embedding model developed for ASM-HEMT
• Modelers invited to provide such tool to PA designers

“PA design is 10 times faster”
Prof. Karun Rawat, IIT Roorkee, India
Nonlinear RF Lab
The Ohio State University
http://www2.ece.ohio-state.edu/~roblin/