The Effect Of non-Rectangular MOS Channels In Modelling High Voltage Lateral MOS

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Introduction

Lateral High Voltage MOS are widely used in Smart Power Technologies, allowing the integration of many different devices in one ASIC.

While typical usage of HVMOS is in power stages, as switches, some circuits need such devices for signals.

In this case, channel length is not minimal and comparable with electrical width. Accurate description of these geometries can be tricky.

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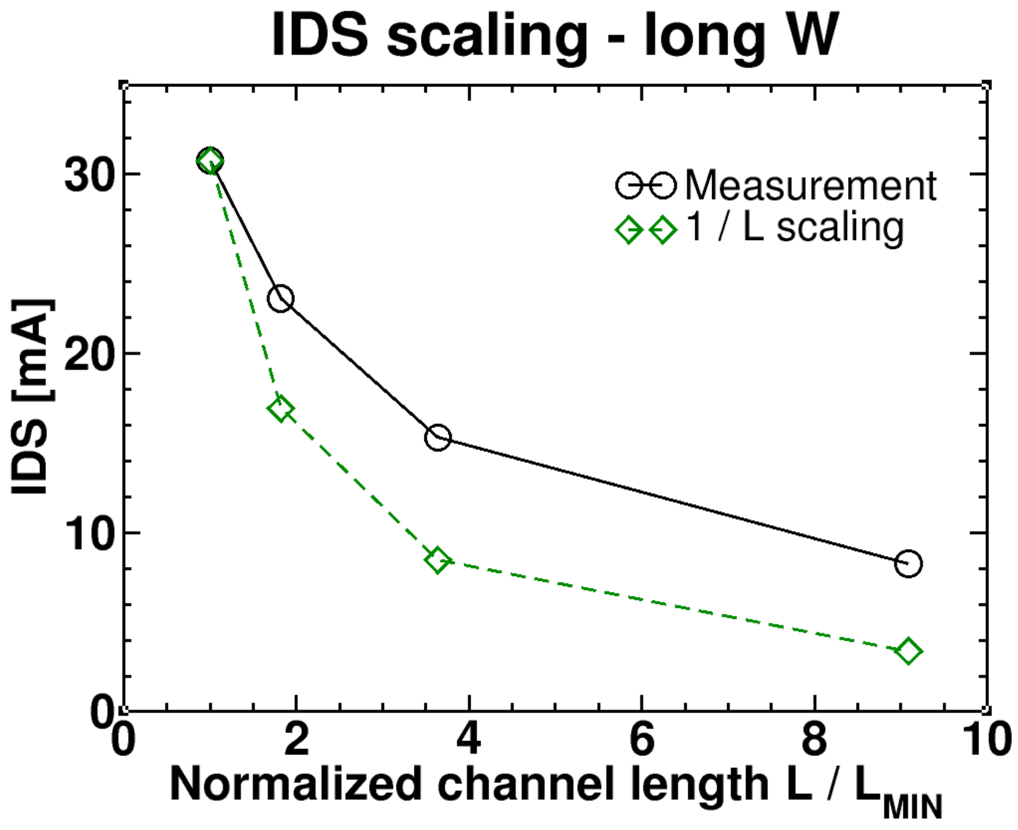
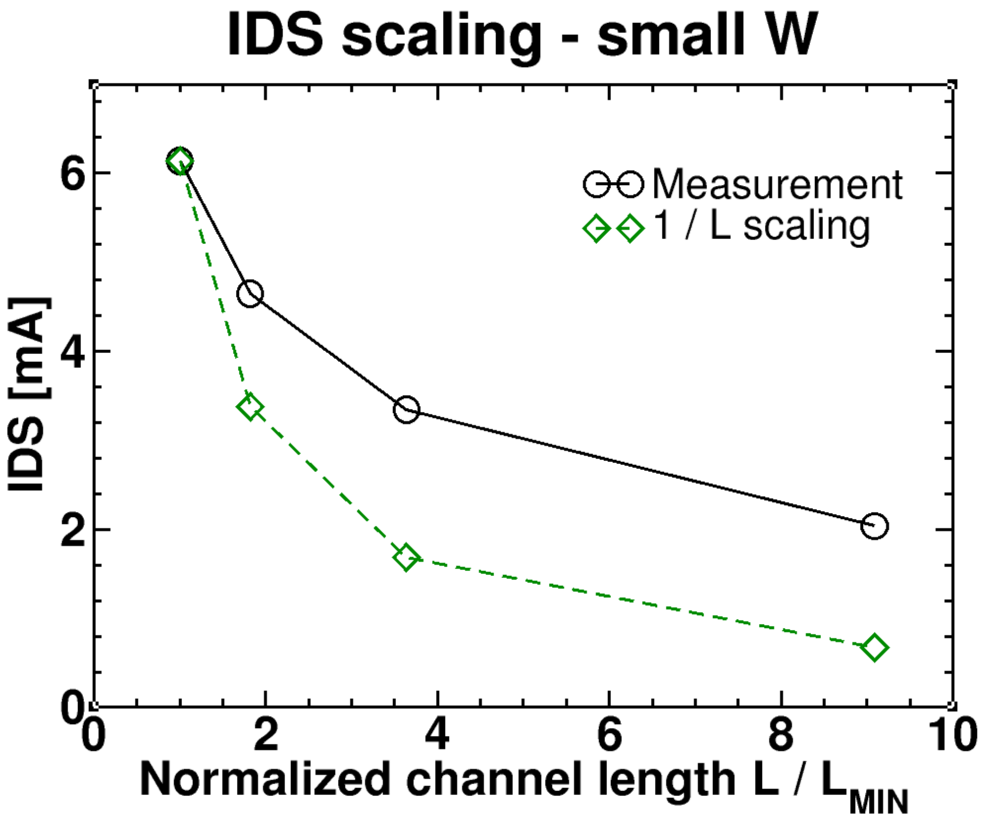
Saturation Current

- Scaling vs channel length





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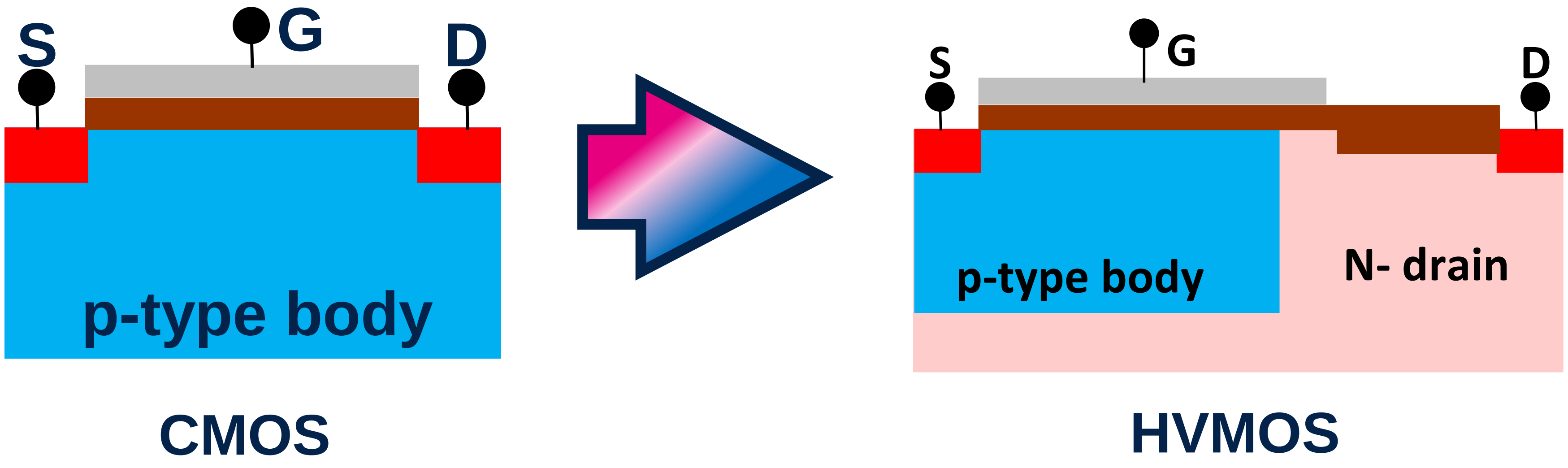
HVMOS

- To guarantee voltage capability, drain is far from source, with field oxide in between.



- Cross sections doesn't explain why scaling with W and L can be different from CMOS.

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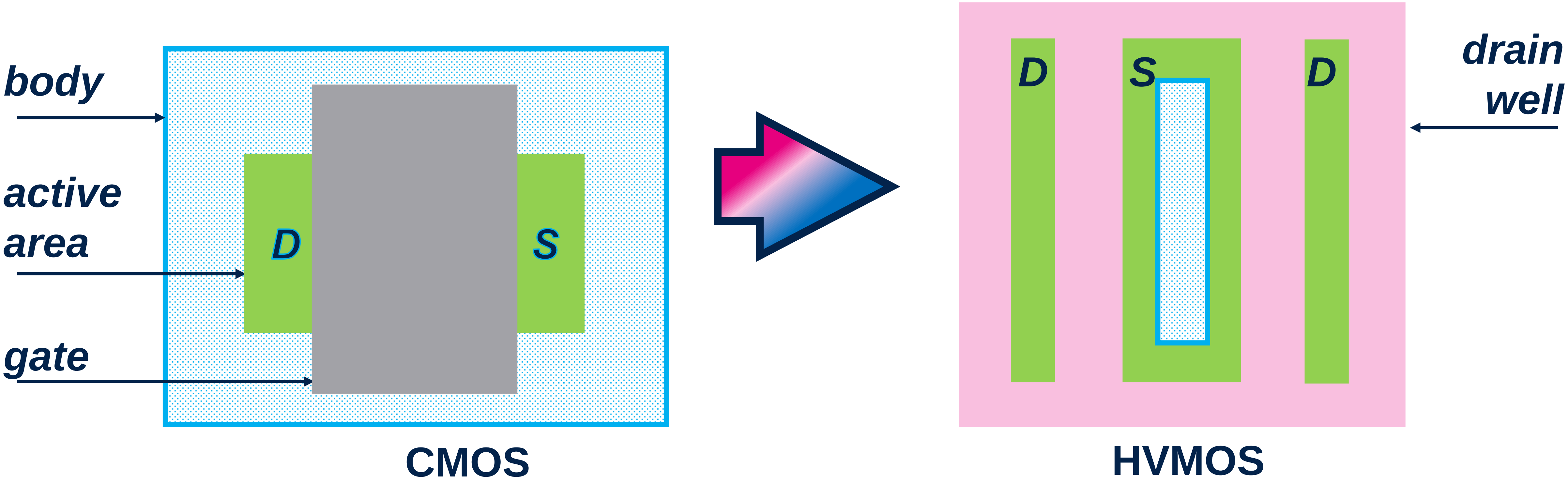
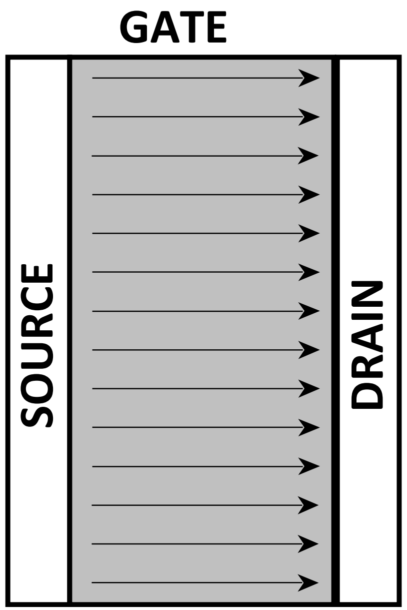
TOP VIEW /1

- Real channel shape is not a rectangle in HVMOS.

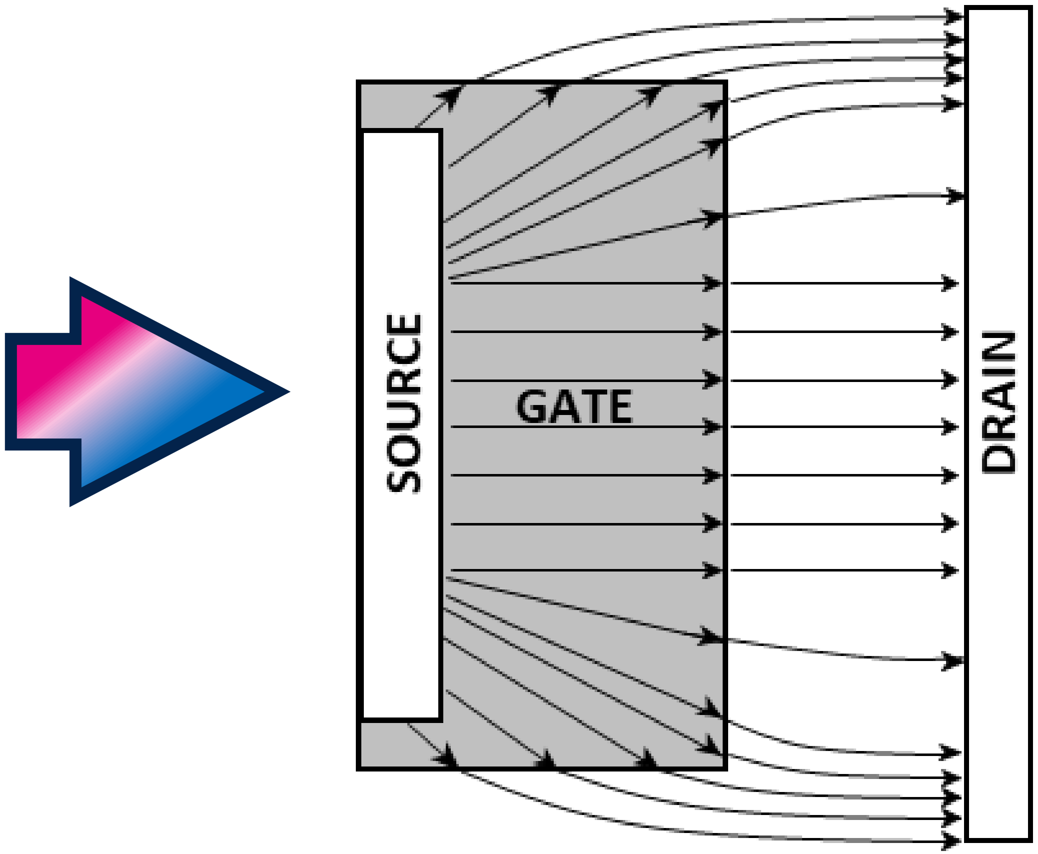


TOP VIEW /2

- Current flow is different



CMOS

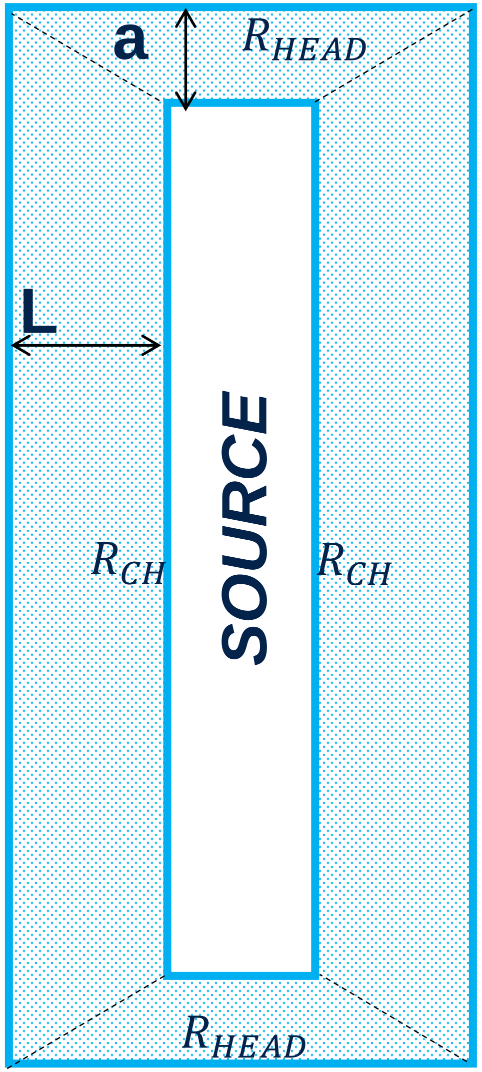


HVMOS

Analytical model /1

- Assumptions:
  - Uniform channel resistivity
  - Potential is constant at body/drain junction

- We have 4 resistor in parallel
  - equal two by two

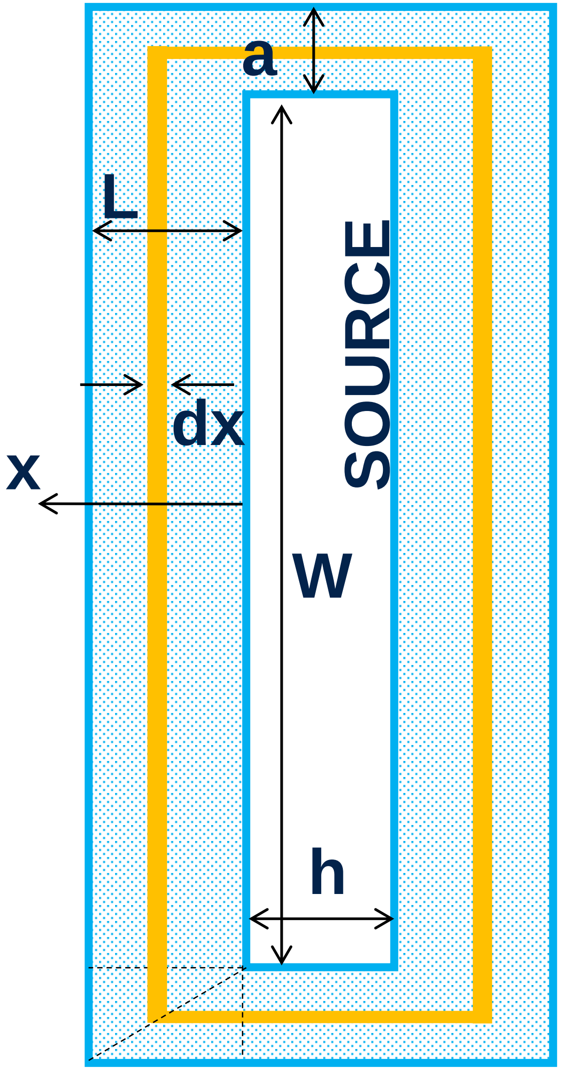


Analytical model /2

- Calculating each infinitesimal piece, we get:

$$dR_{CH} = \rho \frac{\mathrm{d}x}{W + 2\frac{a}{L}x};$$

$$dR_{HEAD} = \rho \frac{\frac{a}{L}\mathrm{d}x}{h + 2x}$$



Analytical model /3

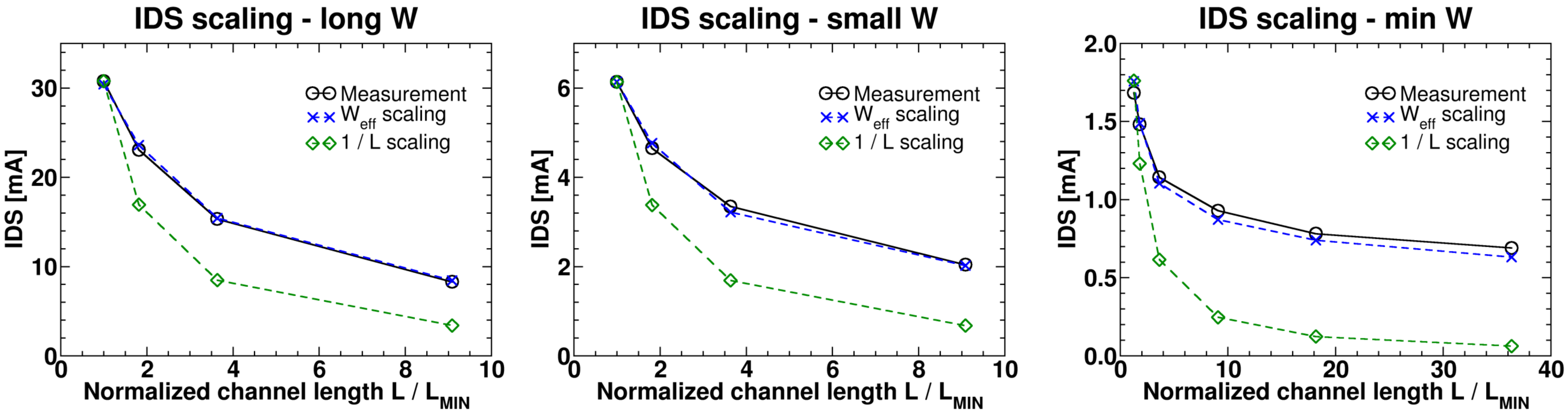
- After some calculations, if we define W_{eff} as $R = \rho\, L/W_{eff}$, we have:

$$W_{eff} = \frac{4kL\left(1 + \frac{L}{a}\right)}{\ln\left[1 + \frac{2k(L + a)}{h + \frac{a}{L}W}\right]}$$

- k is a fitting parameter.

Results

- Using previous formula, outcome is accurate.



- ***W_{eff} curve is the result of a spice simulation***

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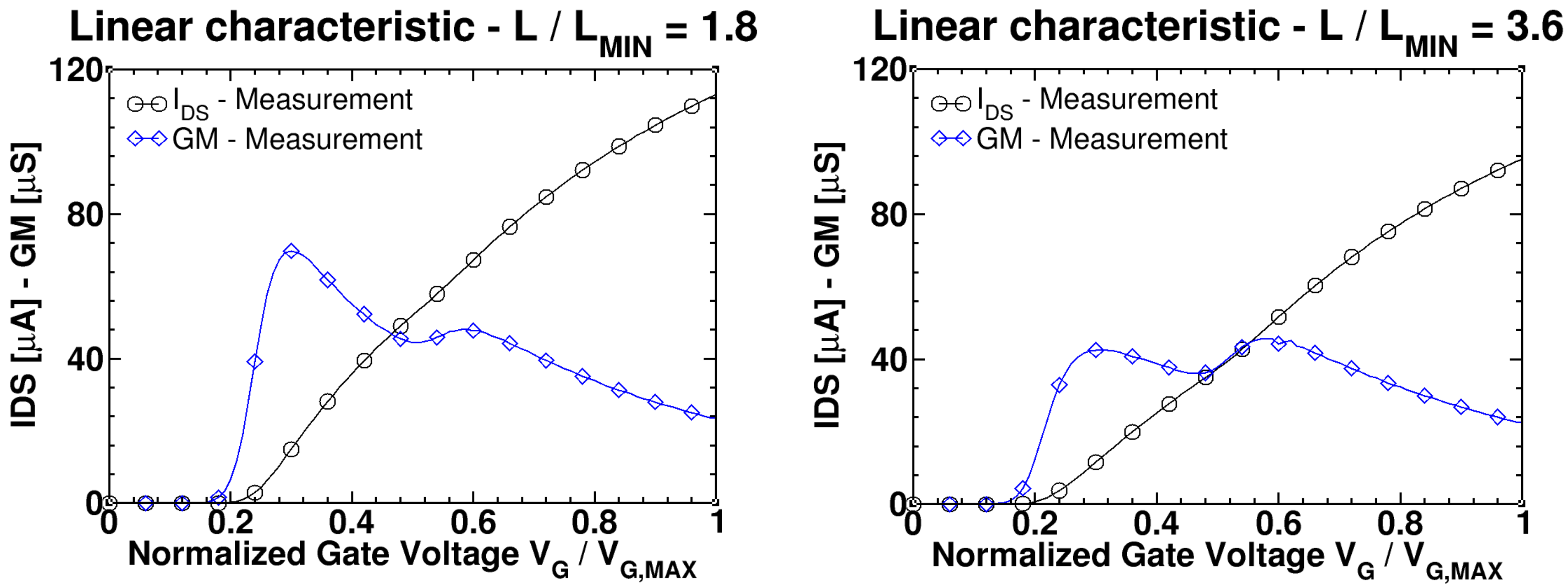
Polysilicon Gate Doping /1

- Some devices has shown a double peak on linear trans characteristic.



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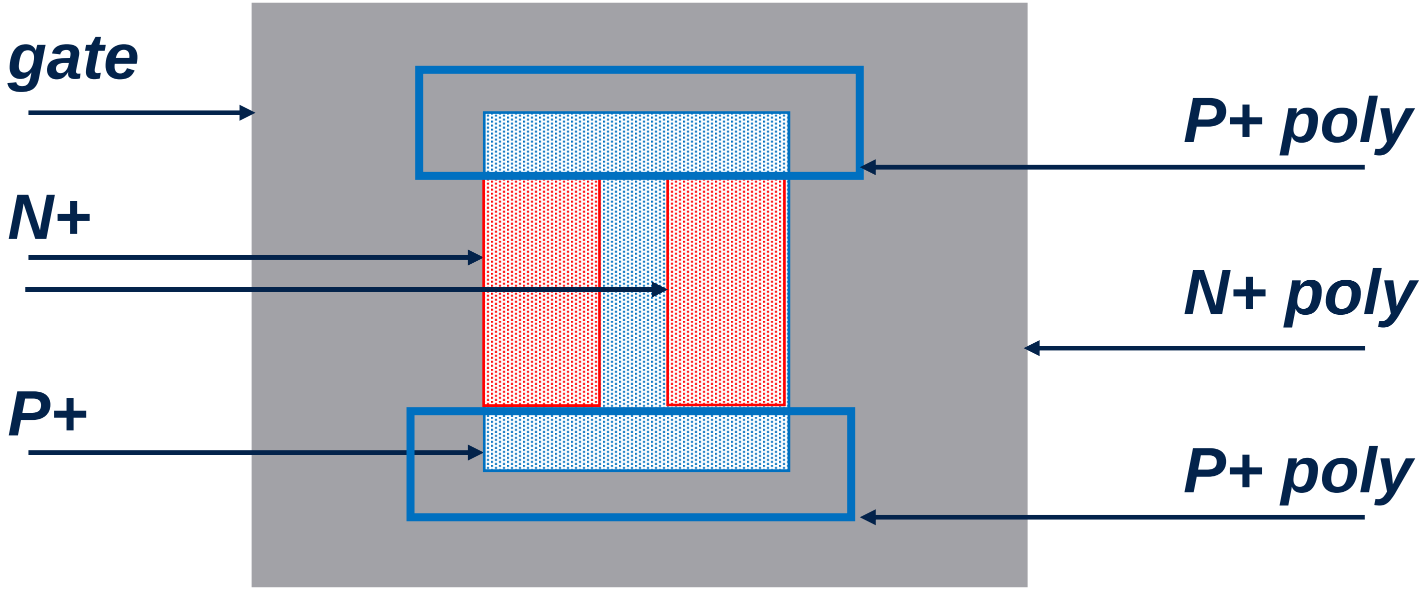
Polysilicon Gate Doping /2

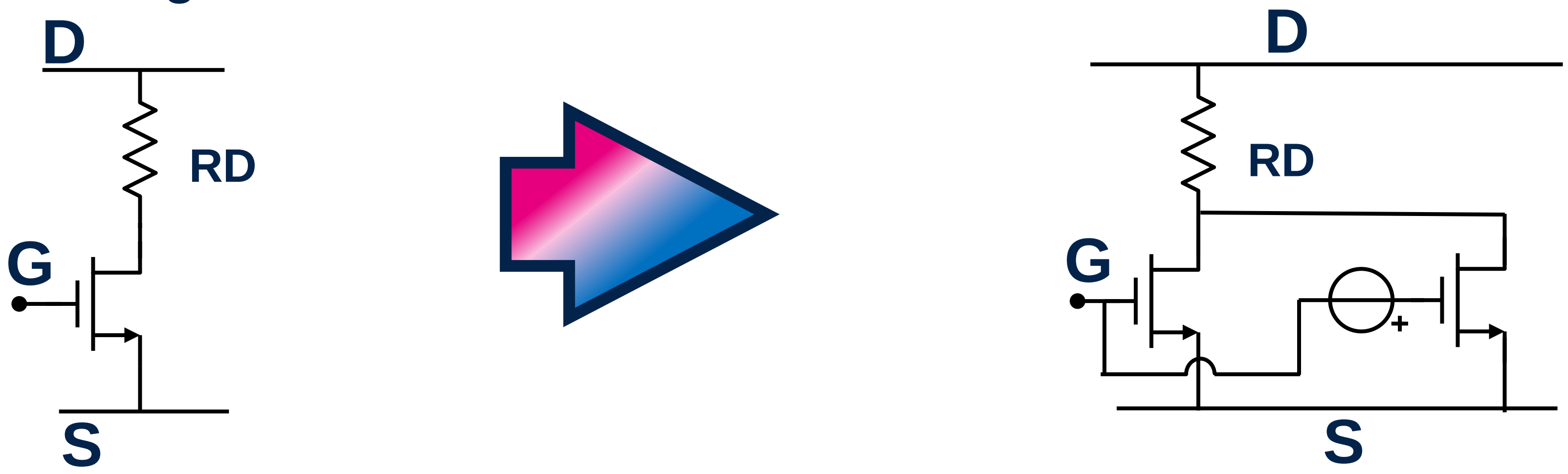
- Another peculiarity of HVMOS is due to source and body contact with a doped poly gate.



HVMOS SOURCE

Polysilicon Gate Doping /3

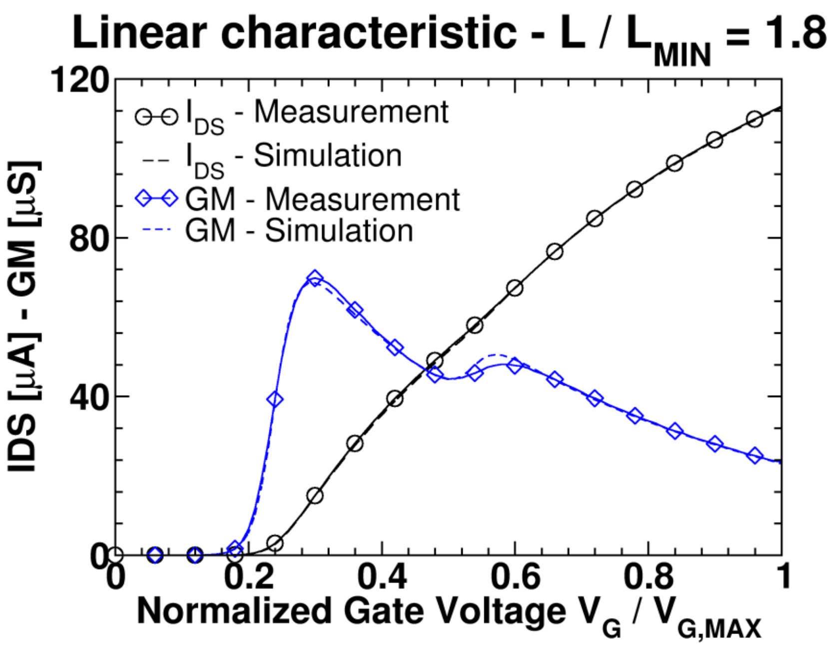
- Origin of the double peak is essentially a parasitic MOS device with a different threshold voltage and fixed size.

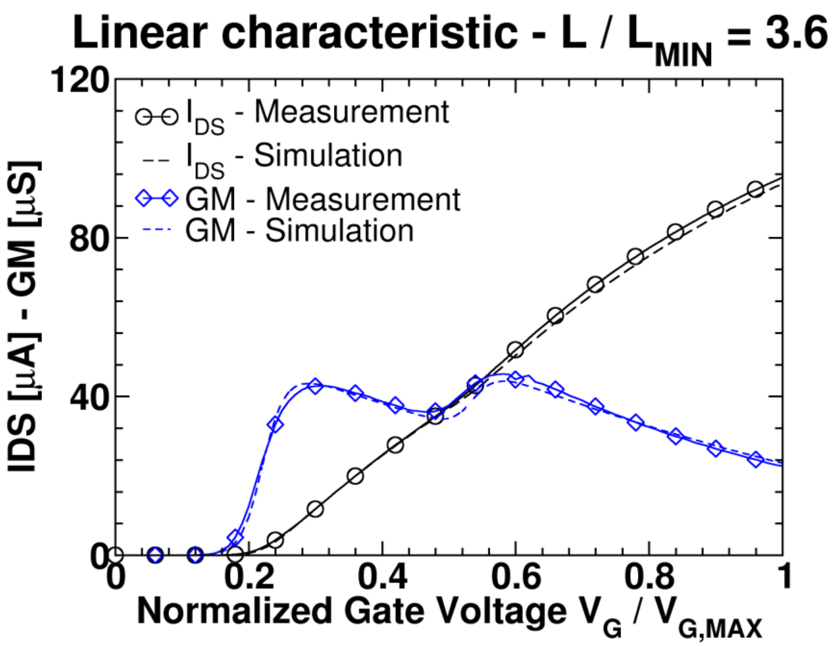


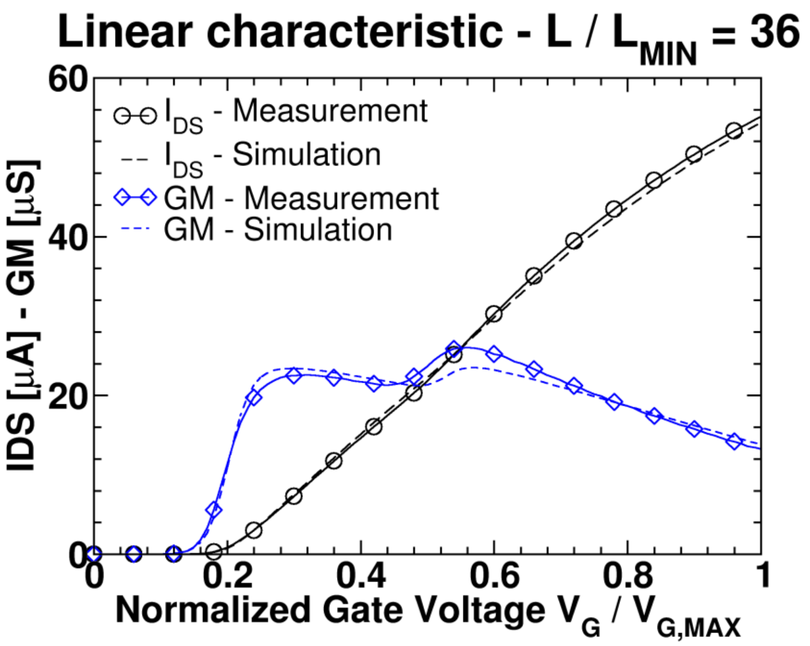
- An empiric solution is to use two instances of the same MOS, one with a modified gate voltage.
- Two fitting parameters
  - DVT: voltage shift of second peak
  - Size of second MOS.

Results

- Using two MOS, result is nice:







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Conclusions

A couple of consequences of not rectangular channels in HVMOS have been presented.

For each effect, a method to deal with it has been described and evaluated versus experimental data.

SOURCE heads

Current may exit laterally changing scaling rule. An analytical approach allow to calculate equivalent size of MOS and reproduce electrical performances.

Different Poly doping on Heads

Double peak on gm can be described with a parasitic MOS with higher V_{TH}.
An empiric solution shows a good agreement Sim vs Exp data.

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Thank you

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