Contact-controlled transistors: Device characteristics and modelling challenges

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Printed and flexible electronics activities growing, on a continuum

EPSRC Fellowship
2021-2026
1. Overview and motivation

2. Contact controlled transistors
   The Source-Gated Transistor – SGT
   The Multimodal Transistor - MMT

3. Device fabrication and characteristics
   The modelling challenge
In many TFT technologies, reducing contact effects is a challenge.

Contact effects reduce current density, transconductance, on-off ratio, cut-off frequency.

But contact effects can also be used constructively.

15+ years of heritage in contact-controlled transistors:
- Source-Gated Transistor (SGT)
- Shannon, Gerstner, Balon, Guo (2003+)
- Sporea (2007+)
- Performance trade-offs

The new multimodal transistor (MMT):
- Sporea and Bestelink (2017+)
- Refines the philosophy
- Higher level of abstraction
Source-gated transistor (SGT) structure

Source-gated transistor (SGT) operation

Source-gated transistor (SGT) operation


\[
V_{SAT} = (V_G - V_{th}) \left( \frac{C_i}{C_i + C_S} \right) + K
\]
Source-gated transistor (SGT) operation


Thermionic-field emission

\[ I_{\text{Mode 1}} = S W A T^2 e^{-\frac{q \Phi_B}{kT}} \]
Source-gated transistor (SGT) operation


\[ I_{\text{Mode 2}} = \int_0^S \frac{V(x)}{R(x)} \, dx \]
Source-gated transistor (SGT) operation

Source-gated transistor (SGT) electrical characteristics

Compared to conventional TFTs:

- Low saturation voltage
- Flat output characteristics
- On-current is lower for the same geometry
- Generally independent of source-drain gap (L)
- Temperature dependence varies with source length (S)
- Field effect mobility cannot be extracted meaningfully because the transport equation is different

As such, conventional TFT/FET models do not apply
The Multimodal Transistor (MMT) Operation
Output and transfer characteristics
The Multimodal Transistor (MMT) Operation

Switching speed

- TFT $V_G = 0.721 \text{ V}$
- SGT $V_G = 10 \text{ V}$
- MMT $V_{CG1&2} = 10 \text{ V}$

$V_{DD} = 10 \text{ V}$

$V_{in}$

$V_{out}$

$C = 1 \text{ fF}$

Gate voltage (mV): 387, 525, 631, 721

1% to final $V_{out}$

Time (ns): $10^1$, $10^2$, $10^3$

Gate voltage (V): 4, 6, 8, 10

$V_D = 10 \text{ V}$

Cut 1

Cut 2

SGT

TFT

MMT
The Multimodal Transistor (MMT)

Operation

Constant transconductance *in saturation*

\[ V_{CG1_{\text{max}}} = 20 \text{ V} \]

step 2 V

<table>
<thead>
<tr>
<th>Drain current (nA)</th>
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<tbody>
<tr>
<td>( V_{\text{DS}} )</td>
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<tr>
<td>( V_{\text{GS}} )</td>
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\[ I_D = \mu_n C_{ox} \frac{W}{L} \left[ V_{DS} (V_{GS} - V_t) - \frac{V_{DS}^2}{2} \right] \]

Ohmic (linear):

\[ V_{GS} > V_t \quad V_{DS} < V_{GS} - V_t \]

Saturation:

\[ V_{GS} > V_t \quad V_{DS} > V_{GS} - V_t \]

\[ I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \]

\[ V_{CG2} = 10 \text{ V} \]

\( W = 50 \mu\text{m} \)

\( S = 54 \mu\text{m} \)

\( d = 18 \mu\text{m} \)

Const. \( g_m \)

Directly proportional

Transconductance (nS)

CG1 voltage (V)

Monday, 14 December 2020
Total gain recovery in floating gate configuration

**The Multimodal Transistor (MMT) Operation**

- **SGT**
  - $V_{G_{\text{max}}} = 10 \text{ V}$
  - step 2.5 V
- **MMT**
  - $V_{C_{G_{\text{max}}}} = 16 \text{ V}$
  - step 4 V

- Floating gate potential for FG1 (source) and FG2 (channel)
  - $V_{C_{G}} = 16 \text{ V}$
  - $V_{C_{G}} = 12 \text{ V}$
  - $V_{C_{G}} = 8 \text{ V}$
  - $V_{C_{G}} = 4 \text{ V}$

- Drain current vs. Drain voltage for SGT and MMT
  - MMT shows improved gain recovery compared to SGT.
The manufacturing challenge has been lowered:
- Staggered electrodes
- Rectifying contacts

Conventional models do not apply directly

Without realistic models, it is hard for designers to adopt these new technologies.

Next: overview of the potential applications
The Multimodal Transistor (MMT)
first publication

COMMUNICATION

28 October 2020

Versatile Thin-Film Transistor with Independent Control of Charge Injection and Transport for Mixed Signal and Analog Computation

Eva Bestelink, Olivier de Sagazan, Lea Motte, Max Bateson, Benedikt Schultes, S. Ravi P. Silva, and Radu A. Sporea*

Microcrystalline silicon
+ Silvaco TCAD
A new Low-complexity Paradigm for Analogue Computation and Hardware learning

NanoRennes / IETR
Silvaco

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2021-2026

Operation and applications of the multimodal transistor
What next?

Let’s talk!
Thank you for your attention!

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