Introducing 3-nm Nano-Sheet technology in Microwind

Etienne SICARD
Professor, INSA, University of Toulouse, France
Etienne.sicard@insa-toulouse.fr

Lionel TROJMAN
Professor, ISEP Paris, France
lionel.trojman@isep.fr
• Context
• Nano-Sheet FET
• 3NM in Microwind
• Examples
• Future

https://hal.archives-ouvertes.fr/hal-03377556
Nano-Sheet (NS), Gate-All-Around (GAA), Muti-Bridge-Channel (MCB), RibbonFET announced in all roadmaps starting 3-NM node.

20-50 times smaller

This Talk
• “The technology node represents the minimum feature size” is **not valid anymore**
Major foundries have announced 3NM, 2NM/20A

- **Gain Space**: 8T, 7T, 5T, 4T, 2T design approaches
- **Improve Speed**: FinFET replaced by Nano-sheet FET
- **Save power**: reduce capacitance, reduce resistance
• IMEC scaling roadmap showing the saturation of horizontal scaling “Contacted Gate Pitch” (CGP), but reduction of cell height (CH)

• Traditional 7 Tracks (7 NM design) vs. 5 tracks (3NM design)
• Less space for internal routing (Dlatch, Complex gates)
• Less space for large width (4-8 $\lambda$, not more)
This talk

**Context**

Improve Speed

---

**MOS FET**

- Gate
- Source
- Drain
- Fin

$W_{eq} = W$

**Fin FET**

- Gate
- Source
- Drain
- Fin

$W_{eq} = 2H + T$

**Nano-Sheet FET**

- Gate
- Source
- Drain
- Nano-sheet

$W_{eq} = 6H + 6T$
We want more current (ION), with less leakage (IOFF), within a reduced silicon area.
3NM vs 5NM

- At the **same frequency**, consume **less power** per stage
- At the **same power** dissipation, go faster

---

http://bsim.berkeley.edu/models/bsimcmg/

BSIM-CMG

BSIM-CMG (Common Multi-Gate) is implemented in Verilog-A. Physically extrinsic models with finite body doping are analyzed analytically with poly-depletion and through a perturbation approach. The performance of the channel doping concentration is improved by setting COREMOD=1.

The important Multi-Gate (MG) transistor behaviors are captured by this model. Volume inversion is included in the solution of Poisson's equation, hence the subsequent I-V formulation automatically captures the volume inversion effect. Analysis of the electrostatic potential in the body of MG MOSFETs provides the model equation for the short channel effects (SCE). The extra electrostatic control from the end-gates (top/bottom gates) (triple or quadruple-gate) is also captured in the short channel model.

See frequently asked questions (FAQ) of BSIM-MG here.

Latest Release

BSIM-CMG 111.1.0 was released on Dec. 8, 2020. It is exclusively available to the CMC members (click here). The open source version will be uploaded here on June 8, 2022.

Download the Previous Versions

- BSIM-CMG 111.0.0 (09/12/2019)

FinFET

Nanosheet
<table>
<thead>
<tr>
<th>Technology node</th>
<th>Year of introduction</th>
<th>Key Innovations</th>
<th>Application note Microwind</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>2003</td>
<td>SOI substrate</td>
<td>hal-03324305</td>
</tr>
<tr>
<td>65nm</td>
<td>2004</td>
<td>Strain silicon</td>
<td>hal-03324309</td>
</tr>
<tr>
<td>45nm</td>
<td>2008</td>
<td>2nd generation strain, 10 metal layers</td>
<td>hal-03324315</td>
</tr>
<tr>
<td>32nm</td>
<td>2010</td>
<td>High-K metal gate</td>
<td>hal-03324299</td>
</tr>
<tr>
<td>20nm</td>
<td>2013</td>
<td>Replacement metal gate, Double patterning, 12 metal layers</td>
<td>hal-03324322</td>
</tr>
<tr>
<td>14nm</td>
<td>2016</td>
<td>FinFET</td>
<td>hal-01541171</td>
</tr>
<tr>
<td>7nm</td>
<td>2017</td>
<td>FinFET Quadruple patterning</td>
<td>hal-01558775</td>
</tr>
<tr>
<td>5nm</td>
<td>2021</td>
<td>FinFET EUV</td>
<td>hal-03254444</td>
</tr>
<tr>
<td>3nm</td>
<td>2021</td>
<td>Nano-sheet FET</td>
<td>hal-03377556</td>
</tr>
<tr>
<td>2nm/20A</td>
<td>2023</td>
<td>NSFet &amp; Buried Power</td>
<td>To appear 2022</td>
</tr>
<tr>
<td>1.5nm/15A</td>
<td>2025</td>
<td>Stacked NSFet, Buried Power</td>
<td>To appear 2022</td>
</tr>
</tbody>
</table>
### 3NM IN MICROWIND DIMENSIONS

- Device dimensions and performances in literature

<table>
<thead>
<tr>
<th>Design parameter</th>
<th>Unit</th>
<th>[Kim 2021]</th>
<th>[Weckx 2019]</th>
<th>[Das 2020]</th>
<th>[Jeong 2020]</th>
<th>[Yoon 2020]</th>
<th>Our choice</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Height</td>
<td>nm</td>
<td>55</td>
<td>60</td>
<td>43</td>
<td>60</td>
<td>50</td>
<td>45</td>
</tr>
<tr>
<td>Gate length</td>
<td>nm</td>
<td>11</td>
<td>15</td>
<td>8, 10</td>
<td>12</td>
<td>12</td>
<td>8</td>
</tr>
<tr>
<td>Nanosheet thickness</td>
<td>nm</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Nanosheet spacing</td>
<td>nm</td>
<td>10</td>
<td>10</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Nanosheet width</td>
<td>nm</td>
<td>24</td>
<td>13</td>
<td>20</td>
<td>42</td>
<td>26</td>
<td>16 (Slow)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>32 (Fast)</td>
</tr>
<tr>
<td>Number of nanosheets</td>
<td></td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>VDD</td>
<td>V</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.7</td>
<td>0.7</td>
<td>0.65</td>
</tr>
<tr>
<td>Ieff nFET</td>
<td>µA</td>
<td>90 (LP)</td>
<td>70</td>
<td>20 (LP)</td>
<td>233 (HP)</td>
<td>30 (LP)</td>
<td>100 (LP-slow)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>180 (HP)</td>
<td>40 (Overdr)</td>
<td></td>
<td>60 (HP)</td>
<td></td>
<td>125 (HP-slow)</td>
</tr>
<tr>
<td>Subthresold slope</td>
<td>mV/Dec</td>
<td>70</td>
<td>75</td>
<td>60-70</td>
<td>100</td>
<td>n.a</td>
<td>60</td>
</tr>
</tbody>
</table>
Fast nsFET $W = 8 \lambda$ (top)
Slow nsFET $W = 4 \lambda$ (bottom)
No restriction on intermediate values
Can be larger than $8 \lambda$
Microwind works in lambda units (\( \lambda \))

Not optimum layout but independent of technology

Very convenient for research & education

Design rules have remained nearly the same for 20 years

\( \lambda \) is 4nm in 3NM (NOT half of technology)

Minimum channel length is 2 \( \lambda \)

Contacted gate pitch (CGP) is 10 \( \lambda \)

Metal pitch (MP) is 6 \( \lambda \) (3+3)
3NM IN MICROWIND
3D VIEW

- D: Dummy Gate
- S: Active Gate
- Fast device
- Slow device
- Nano sheets
• N-Device: Low Power – Slow: \( W_{eq} = 144 \text{nm}, I_{on} = 250 \mu \text{A}, I_{eff} = 100 \mu \text{A}, I_{off} = 0.25 \text{nA} \)
3NM IN MICROWIND DEVICE OPTIONS

- N-Channel NanoSheet device

**Low Power – Slow:**
- $I_{on} = 250 \mu A$
- $I_{off} = 0.25 \text{nA}$

**Low Power – Fast:**
- $I_{on} = 400 \mu A$
- $I_{off} = 0.41 \text{nA}$

**High Performance Fast**
- $I_{on} = 500 \mu A$
- $I_{off} = 4.7 \text{nA (x10 !)}$
• **Contacted Gate Pitch, Metal Tracks**

5 metal tracks (5T)

- **Shared VDD**
- **Track 1**
- **Track 2**
- **Track 3**
- **Track 4**
- **Shared VSS**

**Metal pitch 24 nm**

**Cell height 120 nm**

**CGP 40 nm**

**Contact pitch 40 nm**

**80 nm**

**120 nm**
- Fast and furious mode: Large W, High Power option
- Very short interconnect
Active power per stage (µW)

Ring-Oscillator Frequency per stages (GHz)

- [Ryckaert 2019] 5-nm
- [Samavedam 2020] 5-nm
- [Ahmed 2020] 2-nm @ 0.65V

Nominal VDD (0.65V)
• Role of interconnect delay

**Delay (ps)**

- Interconnect delay
- Gate delay
- Intrinsic delay

**Interconnect load**

- **2 CGP**
  - Short
- **20 CGP**
  - Medium
- **100 CGP**
  - Long

- **CGP = 40 nm (10 λ)**

**Interconnect delay dominates**
**Metal stack**

<table>
<thead>
<tr>
<th>Main target</th>
<th>Pitch</th>
<th>(\lambda)</th>
<th>nm</th>
<th>Used for</th>
</tr>
</thead>
<tbody>
<tr>
<td>M7, M8</td>
<td>4</td>
<td>24</td>
<td>192</td>
<td>Supply</td>
</tr>
<tr>
<td>M5, M6</td>
<td>3</td>
<td>18</td>
<td>144</td>
<td>Long routing</td>
</tr>
<tr>
<td>M3, M4</td>
<td>2</td>
<td>12</td>
<td>96</td>
<td>Medium routing</td>
</tr>
<tr>
<td>M1, M2</td>
<td>1.4</td>
<td>8</td>
<td>64</td>
<td>Short routing</td>
</tr>
<tr>
<td>Gate, Local interc.</td>
<td>1</td>
<td>6</td>
<td>48</td>
<td>Intra-cell routing</td>
</tr>
</tbody>
</table>
• 3NM Nano-Sheet used for the first time at INSA Toulouse for teaching CMOS cell design (Autumn 2021)
• Positive feedback from students
• Easy adaptation to multi-gate technology
• Motivation to design basic blocs for 6G, IA & Ultra-High performance computing chips
• Buried Power Rail (BPR) – IMEC
• Add one routing track for the same cell size


• PowerVia supply using bottom of substrate instead of upper metal layers (2024)

• Similar to IMEC’s buried power rail but generalized to several thick supplies

• Announce for node 20A Intel
• Stacked pFET over nFET: enable 3T design
• Expected for 15A node

• The 3NM Nano-sheet technology has been implemented in Microwind
• Significant gains are observed thanks to cell height reduction and improved efficiency
• Various cell designs have been investigated
• Performances close to available publications
• Successful use for teaching basic cell design for high performance computing
• Further gains expected in 20A and 15A nodes
Thank you for your attention

Etienne.sicard@insa-toulouse.fr
https://hal.archives-ouvertes.fr/hal-03377556
www.microwind.org

Thanks to Wladek Grabinski, MOS-AK, for the invitation to participate to this workshop