Arbeitskreis Modellierung von Systemen und Parameterextraktion
Modeling of Systems and Parameter Extraction Working Group
16th International MOS-AK Workshop
Silicon Valley, December 13, 2023

Enabling Compact Modeling R&D Exchange

European Open Source PDK Initiative

Wladek Grabinski, IEEE EDS DL
MOS-AK (EU)

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Leibniz Institute for High Performance Microelectronics
Frankfurt (Oder)

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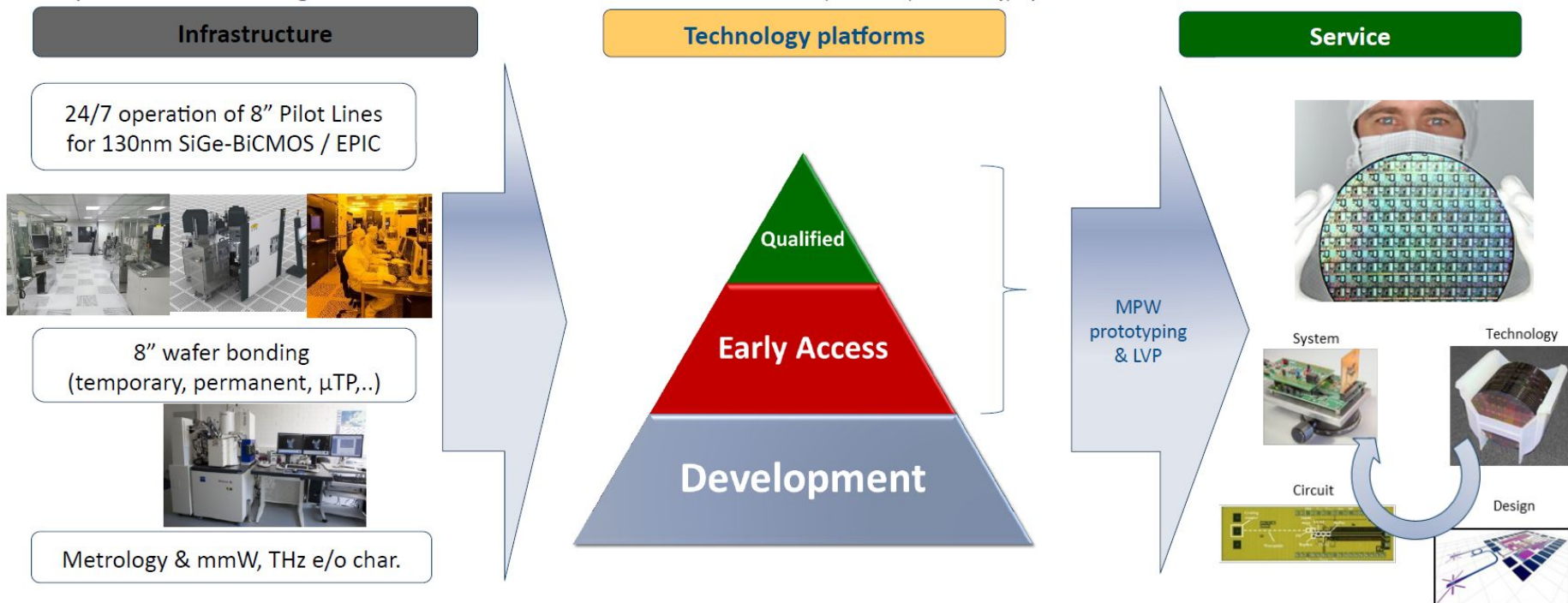
Motivation: A call for Building Talent and Skills

[REF]   EU Chips Act Drives Pan-European Full-Stack Innovation Partnerships
Plenary Session at ISSCC, FEB.20, 2023
Jo De Boeck, Executive VP and CSO, imec & KU Leuven, Belgium

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IHP Institute for High Performance Microelectronics

Infrastructure

24/7 operation of 8" Pilot Lines for 130nm SiGe-BiCMOS / EPIC

8" wafer bonding (temporary, permanent, µTP,..)

Metrology & mmW, THz e/o char.

Technology platforms

Qualified

Early Access

Development

Service

MPW prototyping & LVP

System

Technology

Circuit

Design

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IHP Open PDK & Open Tool Development

- IHP started on existing experiences from SkyWater PDK <https://github.com/google/skywater-pdk

- IHP will offer an analog design flow, later RF design

- Quality should fulfill requirements for academic education

- Open Tools has to be improved, interface development is crucial

- For a sustainable approach, we/IHP have to improve capabilities to a level to support productive projects

- Secure long term funding for MPW and Foundry Service

- Achieve industrial/non-public funding

Digital Open Source Design Flow

The OpenLane Flow
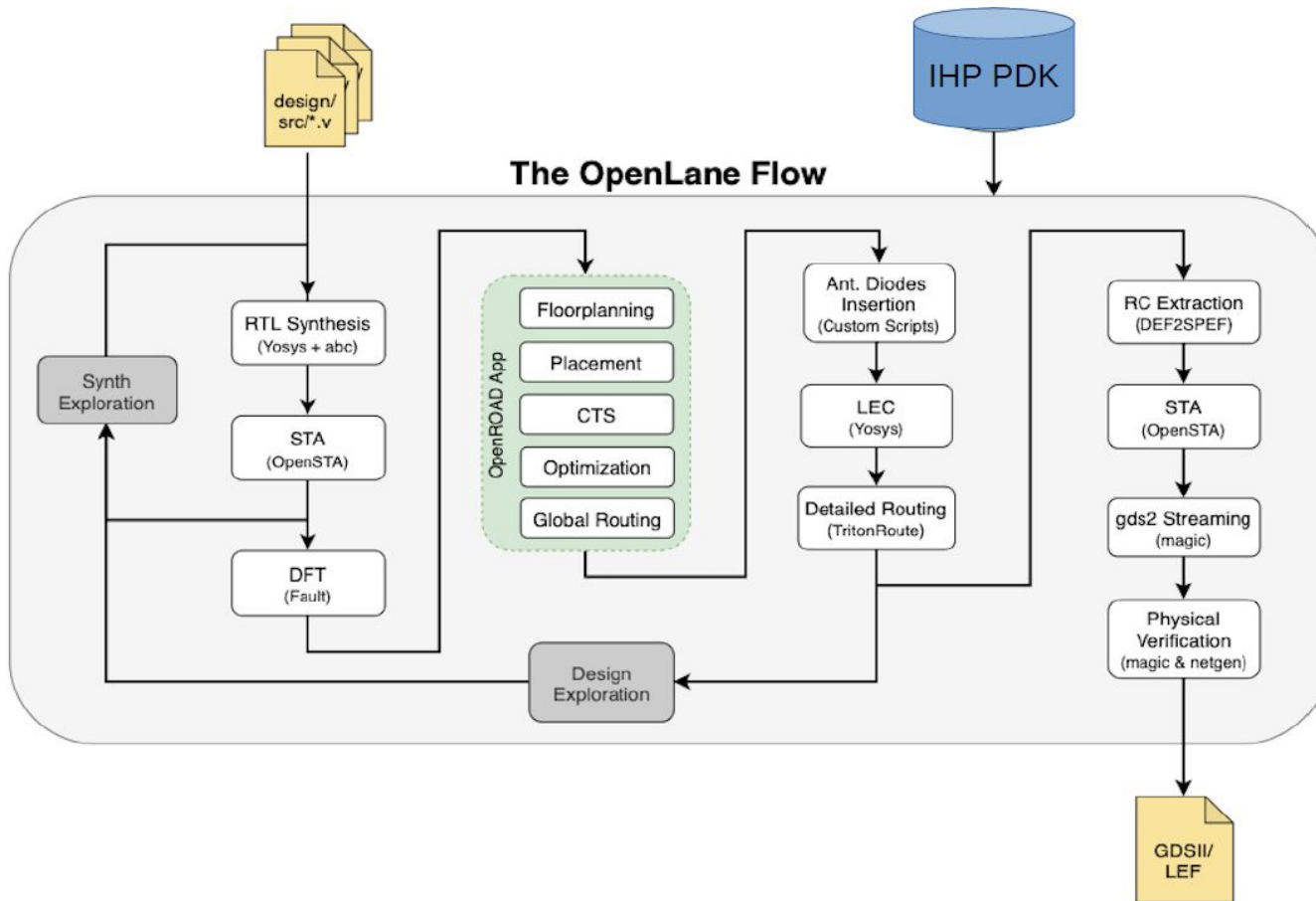
- Yosys + ABC
- Magic
- Netgen
- CVC
- SPEF-Extractor
- OpenSTA
- KLayout
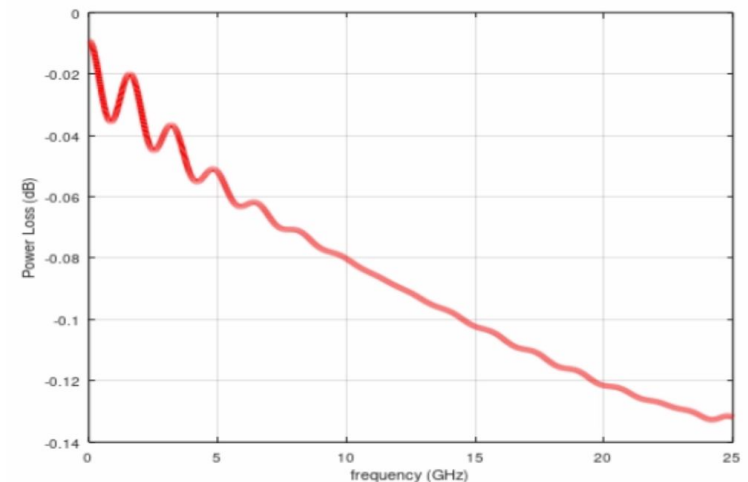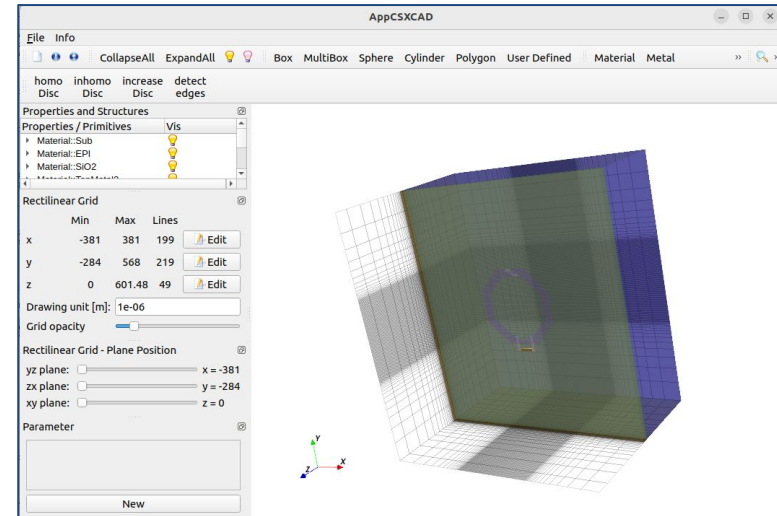- Fast/TritonRoute
- TritonCTS
- other (?)

Analog/RF Open Source Design Flow
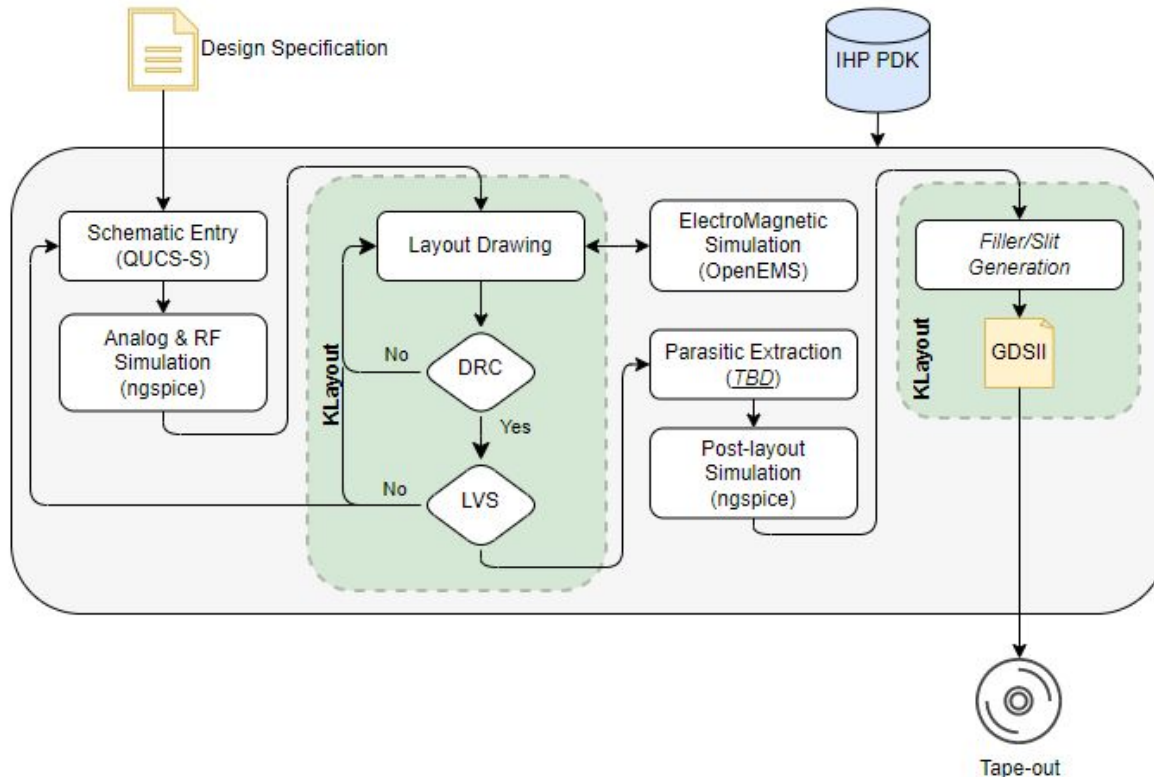
- KLayout-oriented flow
  - Layout design
  - Parameteric cells
  - Physical Verification
- QUCS-S, xschem
- ngspice, xyce
- OpenEMS
- other (?)

OpenEMS ElectroMagnetic Solver

- 3D FDTD solution targeting RF EM simulations
- Model built by Python or Octave scripting
- Graphical viewer for model + mesh (CSXCAD)
- Some interfaces to EDA packages, but no KLayout support yet
- No internal support for GDSII import, interface was created
- using Python library gdspy
- S-Parameter output
- Useful tutorials for RF examples
- Possible issue:
  - small residual energy at low frequency or DC might create DC leakage in simulation results
  - Mostly manual mesh definition
  - No user-friendly GUI for IC designer

QUCS-S Custom Library
with IHP OpenPDK Devices

Iguana - Integrated Systems Laboratory (ETH Zürich)

Iguana: A Linux-Capable Design

- **We choose a complex SoC design**
  - Academy & industry: complexity **increases**
  - More **compute** & **complex interfaces**

- **Evaluating the open flow requires complexity**
  - **Sufficient** hardware **complexity**
    - Full Linux-capable **CVA6** SoC: ~2 MGE
    - Arithmetic operands, std-cell memory, ROMs
    - A **capable** demonstrator chip
  - **Multiple** clock domains (HyperBus, C2C link)
    - Implementation & constraining of CDCs
  - **High-speed**, high-complexity async interfaces
    - Synthesis of DDR/asynchronous logic
   - Constraints and proper setup/hold fixings

AXI X-Bar 64 bit DW 48 bit AW

- LLC / SPM → Hyperbus CTR + PHY
- CVA6
- iDMA
- VGA
- Chip-2-chip Link
- JTAG Debug

Regbus X-Bar 32 bit DW / 48 bit AW
- UART
- SPI
- I2C
- GPIO
- SoC
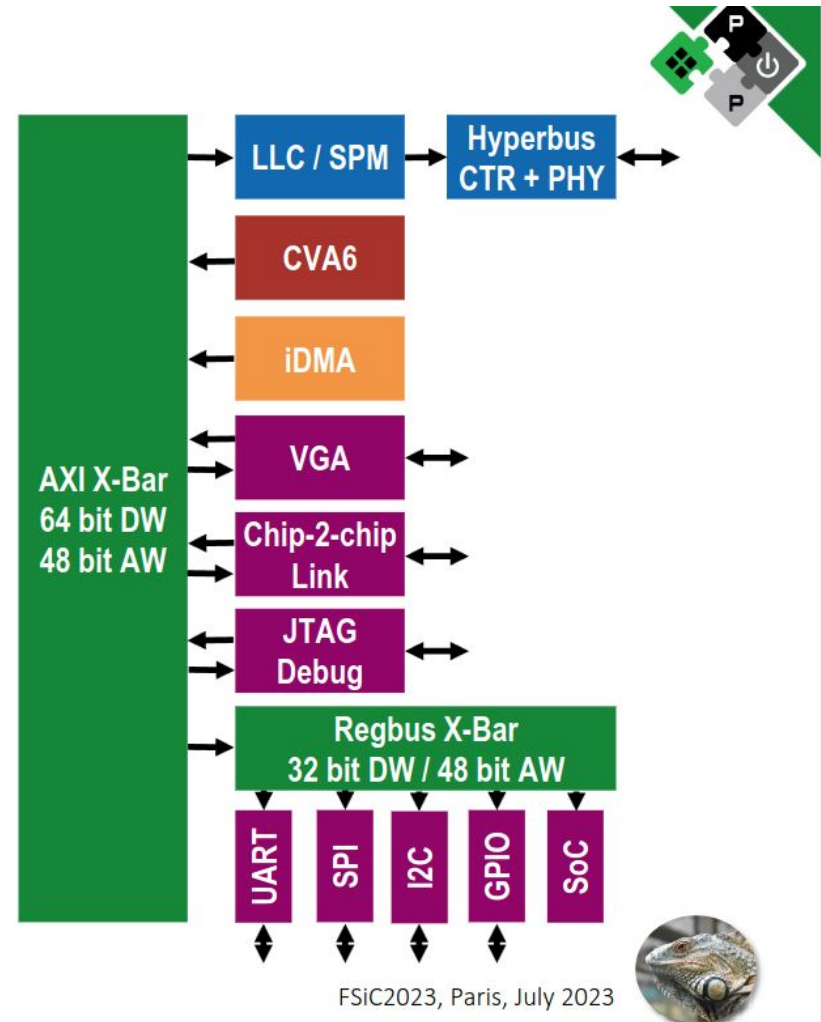
SAR – ADC Project
(JKU Linz)

Design of a 1.2MS/s Charge-Redistribution Non-Binary SAR-ADC utilizing the Open-Source SKY130 PDK

https://github.com/iic-jku/SKY130_SAR-ADC1

- Transfer to open SG13G2 PDK in progress
- Mixed Signal capabilities of open PDK needed
- Both Design Projects can be used to benchmark and optimize open PDK and open Tools
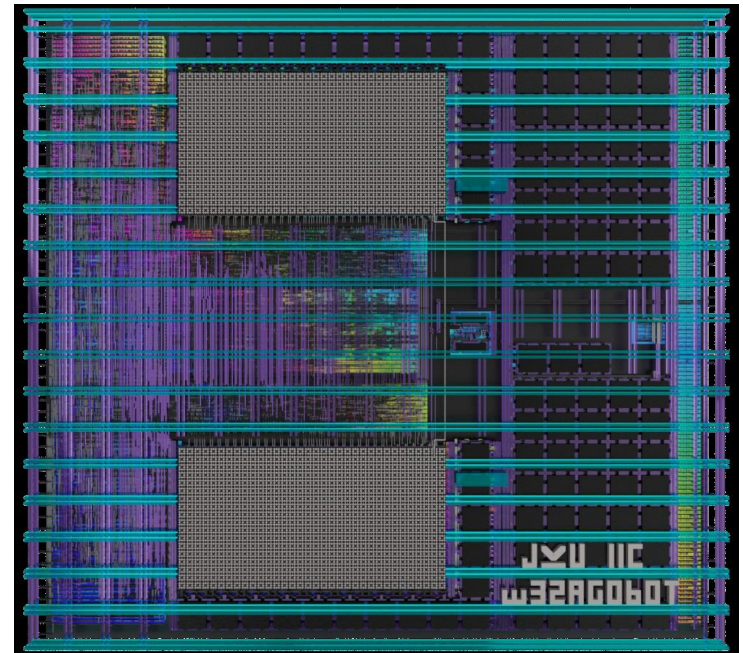
[Note] IIC-OSIC-TOOLS is an all-in-one Docker image for SKY130/GF180/IHP130-based analog and digital chip design
<https://github.com/iic-jku/iic-osic-tools>

IHP Open PDK Roadmap

- Adjust to common goals for an open source design flow – to channel effort
- Leveraging community efforts, public funding and corporate contributions

- Initiate cooperation's and joint projects with open source community
- Demonstration of successful open source designs
- Demonstration of design training courses in academic institutions
- Support chip design possibilities for small commercial design projects
- Achieve a commercial successful project

Acknowledgment

- The IHP PDK Team with Rene Scholz, Open PDK Project Lead
- ETH Zurich + JKU Linz + all the open source community
- German public founded projects:
  - VE-HEP (16KIS1339K) https://elektronikforschung.de/projekte/ve-hep-1
  - IHP Open130-G2 (16ME0852)
  - https://www.elektronikforschung.de/projekte/ihp-open130-g2
  - FMD-QNC (16ME0831)
    https://www.elektronikforschung.de/projekte/fmd-qnc
  - FMD-QNC with VDI/VDE (IHP PDK Workshop funding)