Accurate Modeling of the Self-Heating and Trapping Effects in GaN HEMTs

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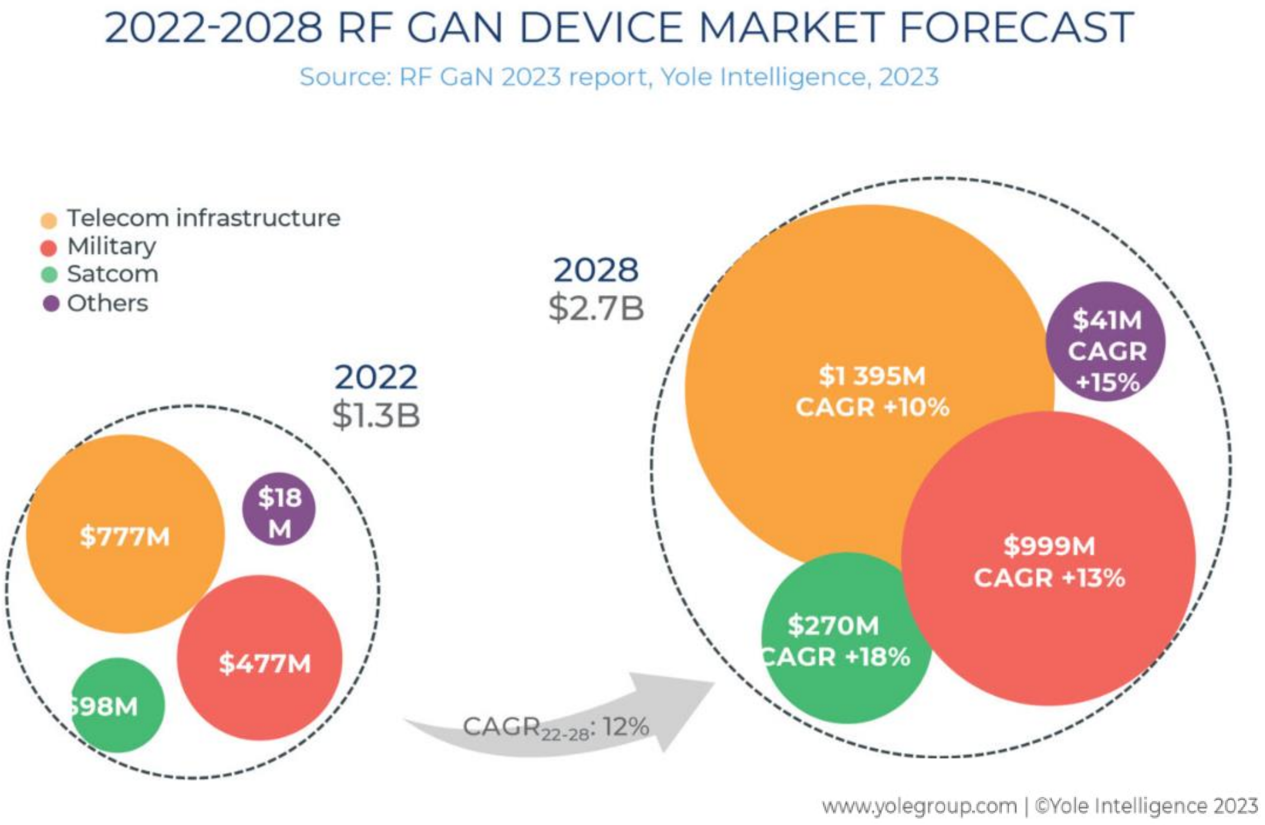
Keysight Technologies

Outline

- **Introduction of GaN HEMTs modeling and new features in ASM-HEMT 101.4 and MVSG_CMC 3.2.0**
- RF parameter extraction package in IC-CAP
  - Parameter extraction flow
  - Thermal extraction
  - Trapping extraction
- Summary

RF GaN is Hot

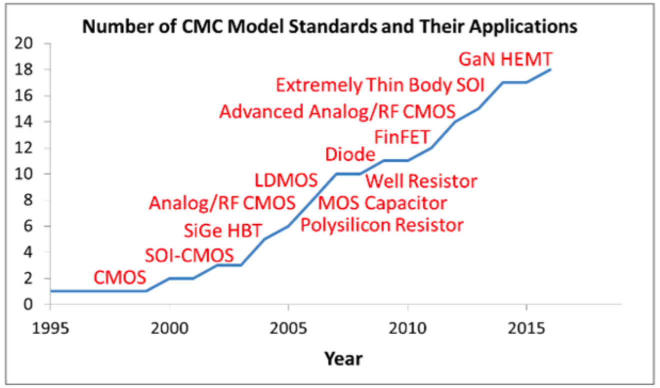
- RF GaN market will grow from $1.3B to $2.7B by 2028



Source: “RF GaN market broadens its appeal with an appetite for GaN-on-Silicon” - www.yolegroup.com

GaN Model Development History

CMC
SPICE
Standards
Compact Model
Coalition



ASM-HEMT 101.4

MVSG_CMC 3.2.0

Phase 1
- 8 candidates
- Accuracy
- Convergence
- Physical nature

Phase 2
- 4 candidates
- Sponsors
- Data

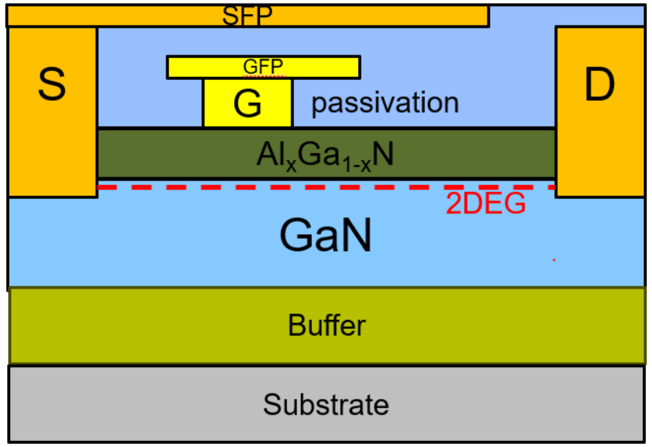
Phase 3
- 2 candidates
- Model evaluation
- Feedback

Phase 4
- Model support
- Version release

Source: “RF GaN market broadens its appeal with an appetite for GaN-on-Silicon” - www.yolegroup.com

Modeling of Various GaN Device Effects

- **Field-plates** – modeled with computationally efficient formulation
- **Non-linear access region** – physics-based formulation covering linear and saturation
- **Gate-current (IG)** – physics-based formulations covering multiple IG mechanisms
- **Trapping effects** – multiple modes to suit applications and extraction flows
- **Noise** – Physics-based thermal- and flicker noise models
- **Self-heating effect** – modeled with thermal sub-circuits
- **Ambient temperature effects** – modeled with temperature-dependent formulations
- …



All effects modeled with consistency with each-other

Source: Sourabh Khandelwal, “Scalable nonlinear RF modeling of GaN HEMTs with industry standard ASM-HEMT compact model - Enabling new modeling capabilities for GaN” - IMS

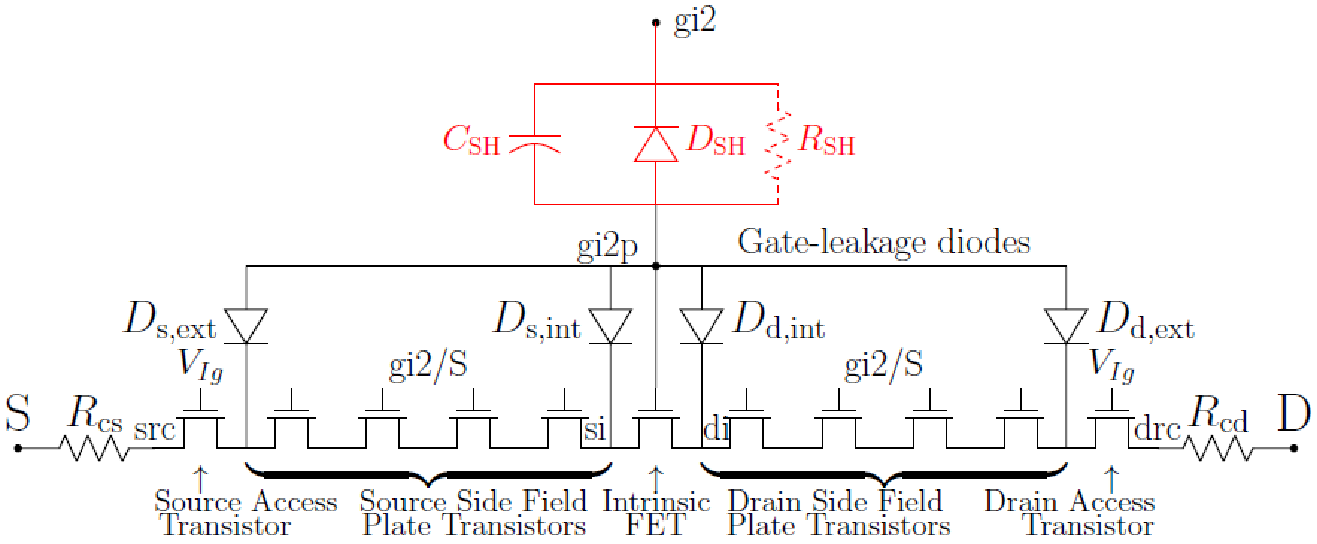
ASM-HEMT 101.4 New Features

- New current saturation formulation added to the access region resistance model
- Two new model parameters tepi and asub added to tune the substrate voltage dependence of pinch-off voltage
- Technical manual updated with new section 5.2 describing statical model extraction flow

Source: Release notes of ASM-HEMT 101.4

MVSG_CMC 3.2.0 New Features

- External thermal node added – additional temperature offset can be defined at the netlist level
- Schottky p-GaN implementation to include dynamic Vt effect



Source: release notes of MVSG_CMC 3.2.0

Outline

- Introduction of GaN HEMTs modeling and new features in ASM-HEMT 101.4 and MVSG_CMC 3.2.0
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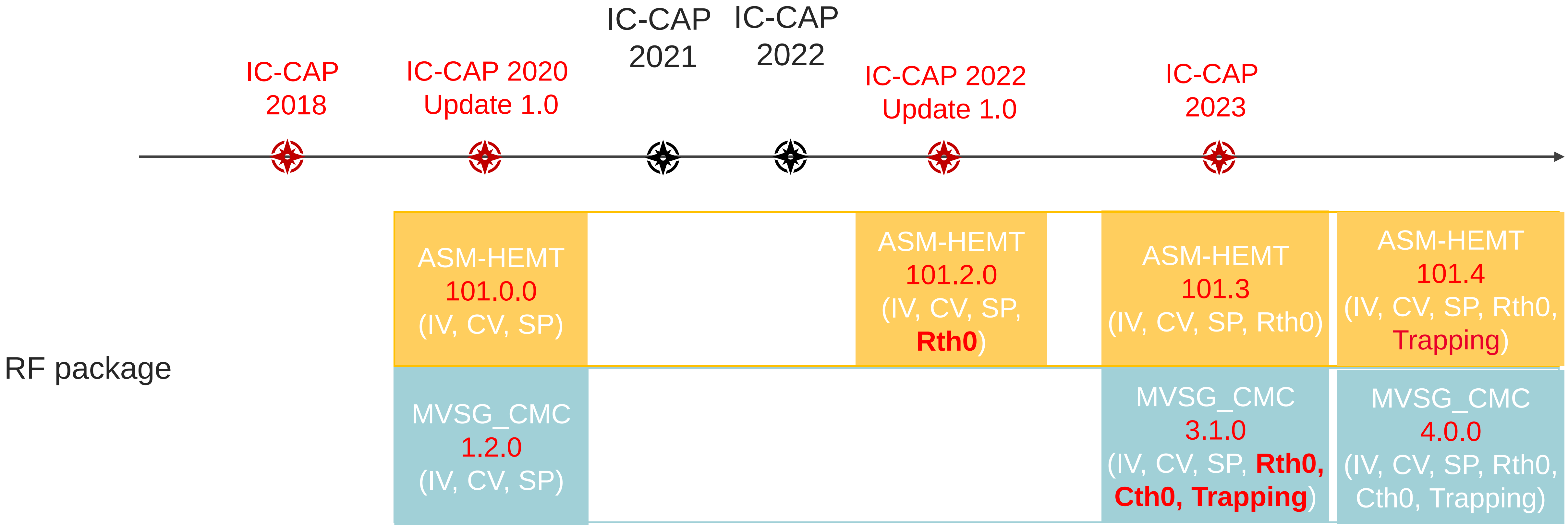
ASM and MVSG Modeling Packages Updates in IC-CAP



IC-CAP 2018

IC-CAP 2020 Update 1.0

IC-CAP 2021

IC-CAP 2022

IC-CAP 2022 Update 1.0

IC-CAP 2023

RF package

ASM-HEMT
101.0.0
(IV, CV, SP)

MVSG_CMC
1.2.0
(IV, CV, SP)

ASM-HEMT
101.2.0
(IV, CV, SP, **Rth0**)

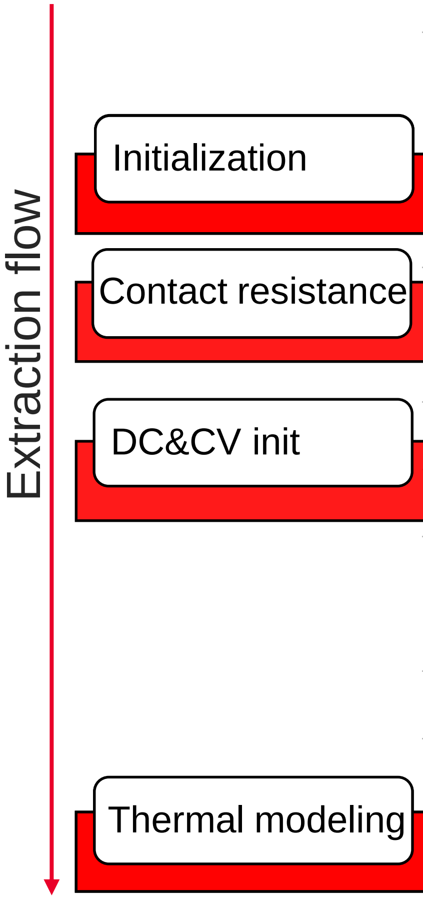
ASM-HEMT
101.3
(IV, CV, SP, Rth0)

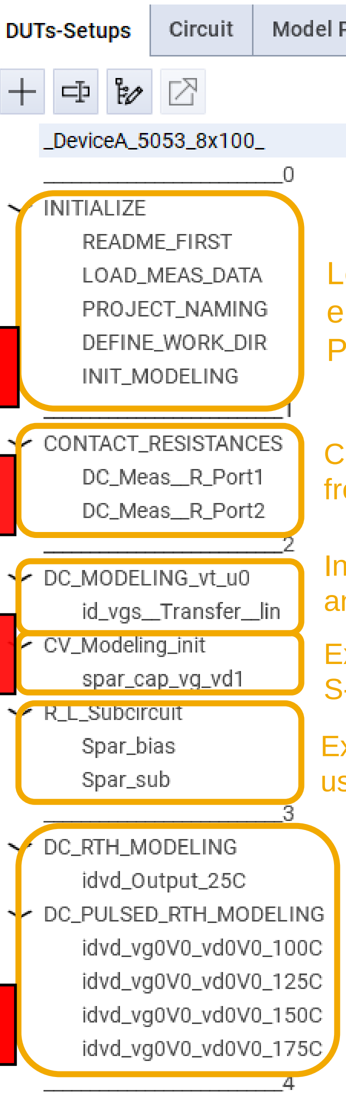
MVSG_CMC
3.1.0
(IV, CV, SP, **Rth0, Cth0, Trapping**)

ASM-HEMT
101.4
(IV, CV, SP, Rth0, Trapping)

MVSG_CMC
4.0.0
(IV, CV, SP, Rth0, Cth0, Trapping)

Modeling Flow (ASM-HEMT)





_DeviceA_5053_8x100_

0

INITIALIZE
  README_FIRST
  LOAD_MEAS_DATA
  PROJECT_NAMING
  DEFINE_WORK_DIR
  INIT_MODELING

1

CONTACT_RESISTANCES
  DC_Meas__R_Port1
  DC_Meas__R_Port2

2

DC_MODELING_vt_u0
  id_vgs__Transfer__lin
CV_Modeling_init
  spar_cap_vg_vd1
R_L_Subcircuit
  Spar_bias
  Spar_sub

3

DC_RTH_MODELING
  idvd_Output_25C
DC_PULSED_RTH_MODELING
  idvd_vg0V0_vd0V0_100C
  idvd_vg0V0_vd0V0_125C
  idvd_vg0V0_vd0V0_150C
  idvd_vg0V0_vd0V0_175C

4

Load Meas Data/Setup environment/Model Parameter initialization

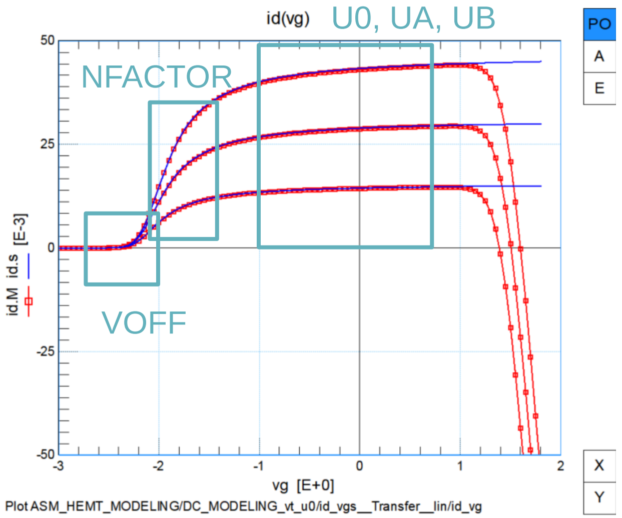
Contact resistance from the probe

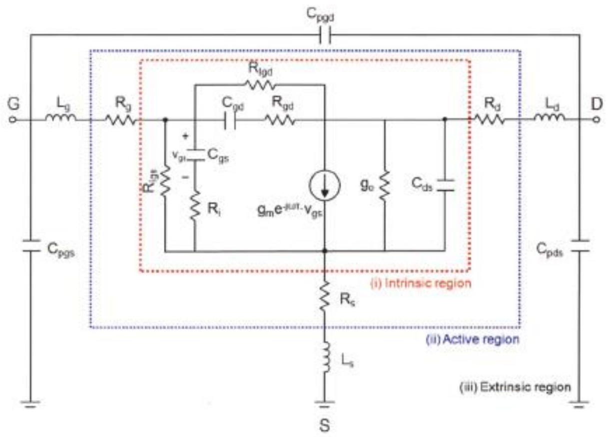
Initial threshold voltage and mobility

Extract cap by using S-parameters

Extract parasitics using S11 and S22

Self-heating extraction with static and pulsed IV

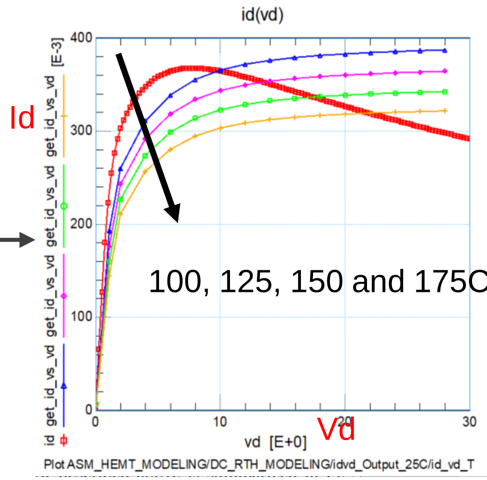


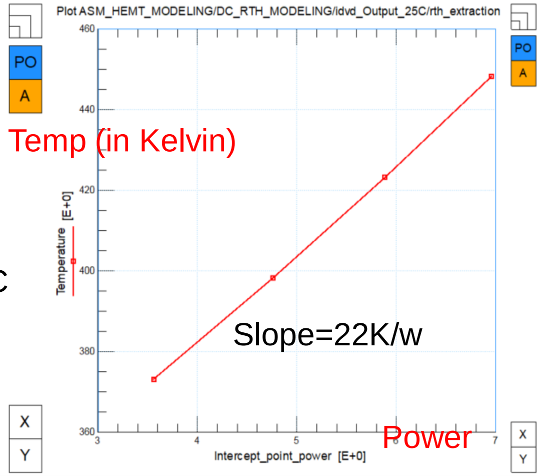


$$C_{gs} = \frac{Im(Y_{11})+Im(Y_{12})}{\omega}\left[1+\left(\frac{Re(Y_{11})+Re(Y_{12})-g_{lgs}}{Im(Y_{11})+Im(Y_{12})}\right)^2\right]$$

$$C_{gd} = -\frac{Im(Y_{12})}{\omega}\left[1+\left(\frac{Re(Y_{12})+g_{lgd}}{Im(Y_{12})}\right)^2\right]$$

$$C_{ds} = \frac{Im(Y_{22})+Im(Y_{12})}{\omega}$$





Modeling Flow (ASM-HEMT)

Extraction flow

Continues IV for DC modeling & Temperatures

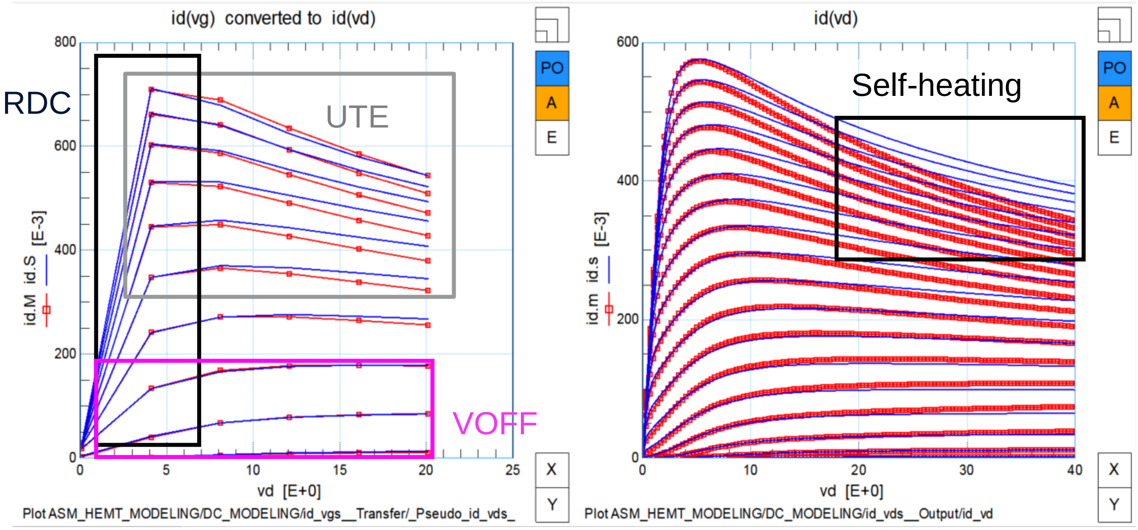
- DC_MODELING
  - ig_vgs__Input
  - id_vgs__Transfer__lin
  - id_vgs__Transfer_subVOFF
  - id_vgs__Transfer
  - id_vds__Output

Extract DC parameters and RTH0

- DC_MODELING_TEMP
  - id_vds__Output__m25C
  - id_vds__Output__25C
  - id_vds__Output__75C
  - id_vds__Output__100C

5

Extract thermal parameters with IdVd at different temperatures



CV modeling

- CV_Modeling
  - spar_cap_vd_vglow
  - spar_cap_vg_vd1
  - spar_cap_vd_vg_T
  - spar_cap_vg_vdhigh

6

Extract cap parameters at low voltage and thermal parameters at high voltage

- DC_MODELING_LSYNC
- DC_PULSED
- DC_ModelRobustness

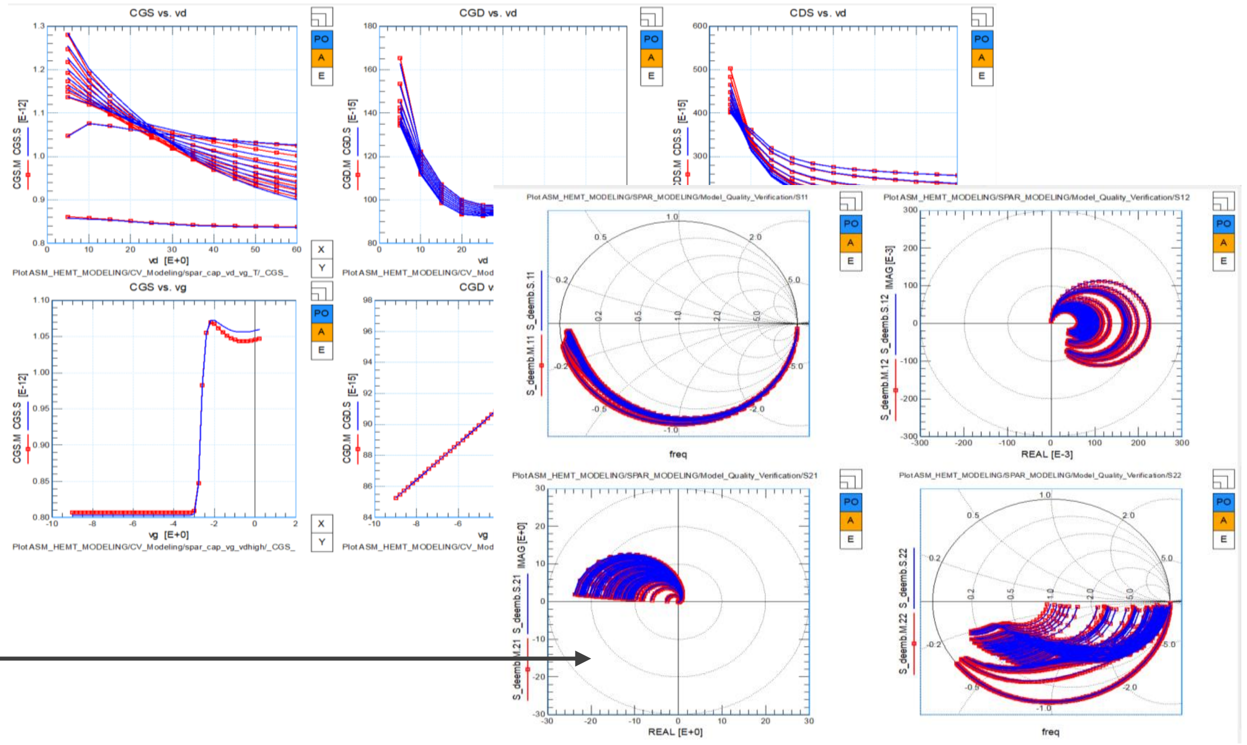
7

S-parameters

- SPAR_MODELING
  - Init_Spar_Modeling
  - vg_1stsweep__vd_2nd
  - vd_1stsweep__vg_2nd
  - Spar_all_freq_biases
  - Spar_bias_point
  - Model_Quality_Verification

8

Extract parasitic effect (LG, LD, LS, RG)



Trapping modeling

- TRAPPING_MODELING
  - pulsed_vd_50
  - pulsed_vd_40

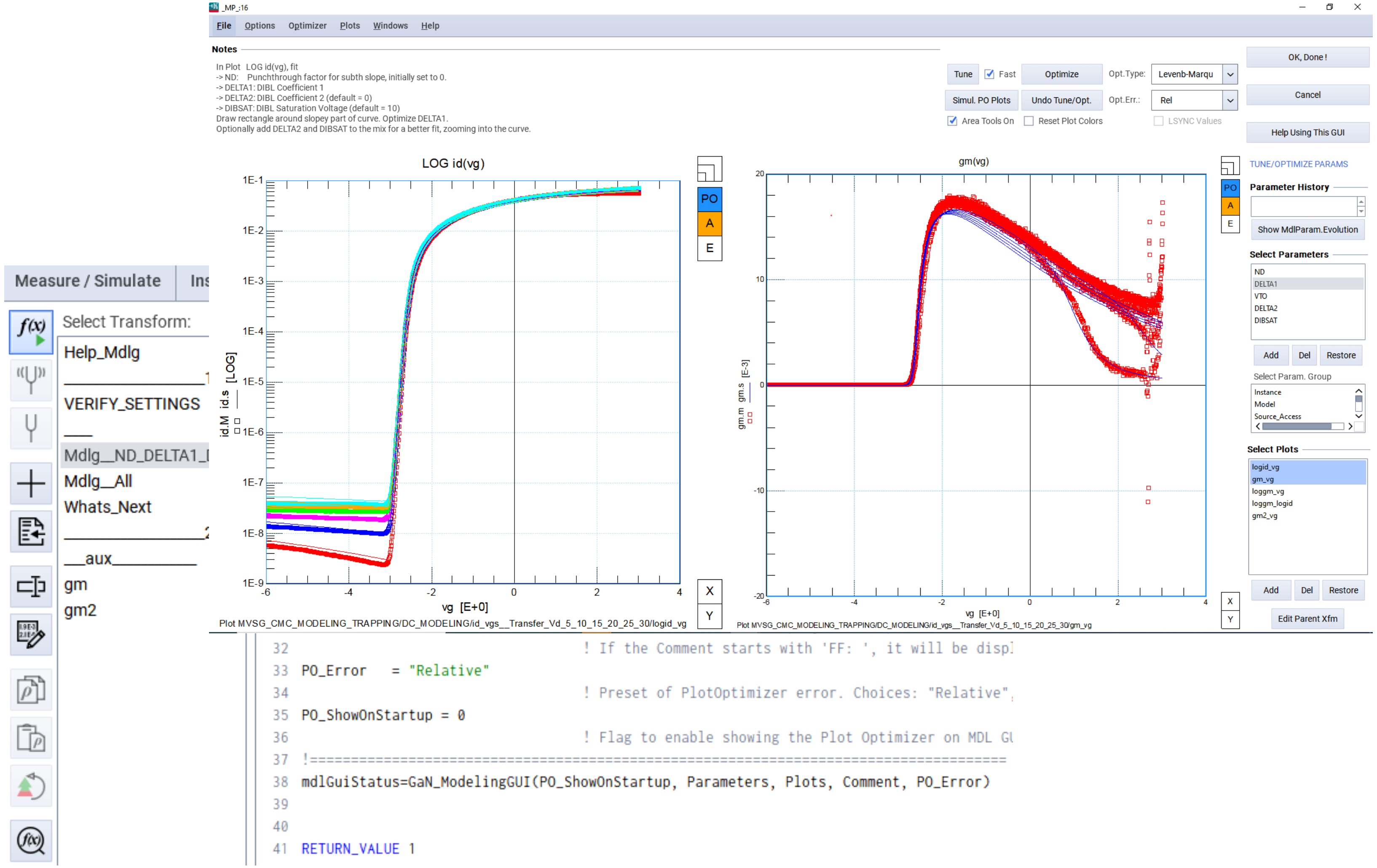
Gate-lag and drain-lag

KEYSIGHT

MVSG_CMC Parameter Extraction in IC-CAP

- Contact Resistances
- Capacitance vs. Voltage
- Pulsed IV for DC
- Thermal Sub Circuit
- S-Parameters
- Trapping Module
- Large Signal Power

UTILITIES: provide GUI and function to help modeling



Opt.Type: Levenb-Marqu

Opt.Err.: Rel

In Plot LOG id(vg), fit
-> ND: Punchthrough factor for subth slope, initially set to 0.
-> DELTA1: DIBL Coefficient 1
-> DELTA2: DIBL Coefficient 2 (default = 0)
-> DIBSAT: DIBL Saturation Voltage (default = 10)
Draw rectangle around slopey part of curve. Optimize DELTA1.
Optionally add DELTA2 and DIBSAT to the mix for a better fit, zooming into the curve.

Plot MVSG_CMC_MODELING_TRAPPING/DC_MODELING/id_vgs__Transfer_Vd_5_10_15_20_25_30/logid_vg

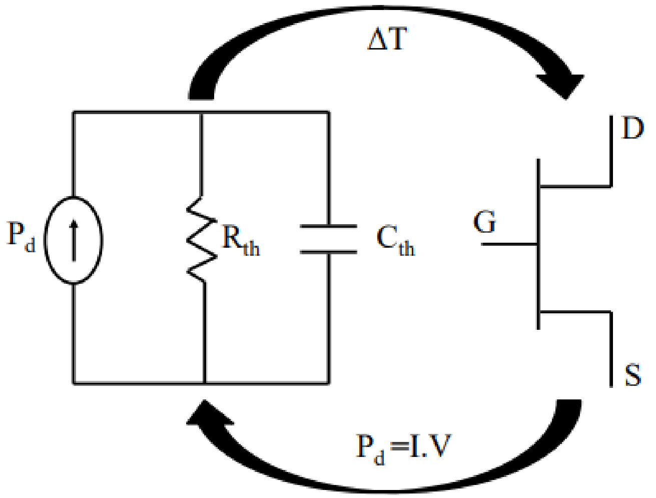
Plot MVSG_CMC_MODELING_TRAPPING/DC_MODELING/id_vgs__Transfer_Vd_5_10_15_20_25_30/gm_vg

```
                                        ! If the Comment starts with 'FF: ', it will be disp
PO_Error    = "Relative"
                                        ! Preset of PlotOptimizer error. Choices: "Relative",
PO_ShowOnStartup = 0
                                        ! Flag to enable showing the Plot Optimizer on MDL G
!=================================================================================
mdlGuiStatus=GaN_ModelingGUI(PO_ShowOnStartup, Parameters, Plots, Comment, PO_Error)


RETURN_VALUE 1
```

Self-Heating Effect

- Self-heating effect has become a greater concern for industry in recent years. Since smaller devices, new materials and geometries, resulting in an increase of this effect.
- Self-heating results in an increase of the device temperature will cause mobility reduction, compromised reliability and signal delays.
- In ASM-HEMT and MVSG_CMC models, self-heating effect is modeled by standard R-C network, which contains thermal resistance RTH0 and thermal capacitance CTH0.

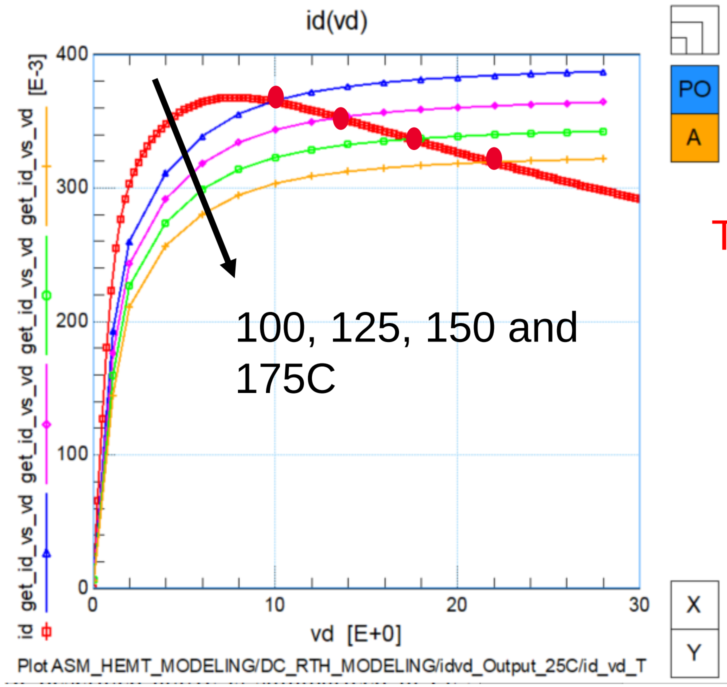


Source: S. Khandelwal et al., " ASM-HEMT 101.2.0 Advanced SPICE Model for HEMTs," Technical Manual [2020].

Self-heating Extraction

- We need two types of data:
  - Static IdVd at room temperature.
  - Pulsed IdVd at various other than the room temperature.
  - Vd0=0V and Vg0=0V, which are the voltage at low level.

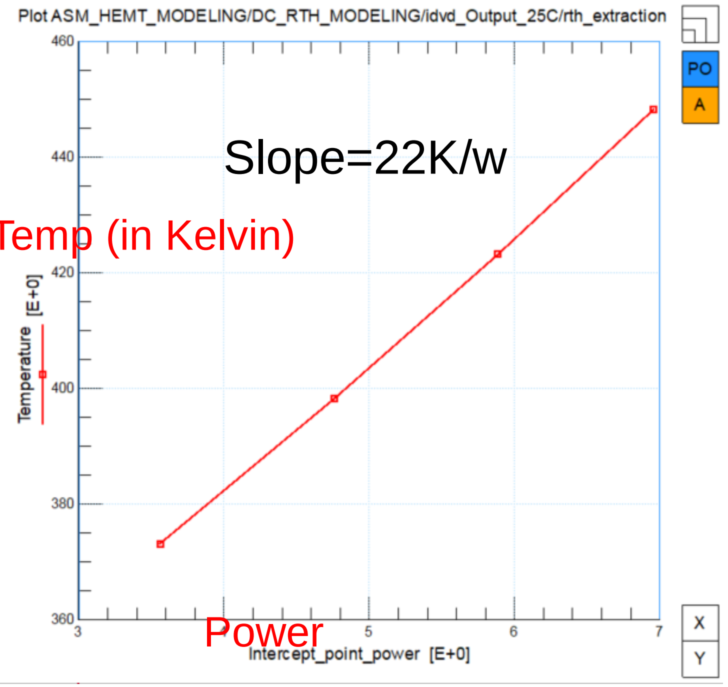
DC, T1=25C
Pulsed from (0,0), T2=100C
DC curve: $T1 = T1_{ambient} + RTH0 \cdot P_{diss1}$
Pulsed curve: $T2 = T2_{ambient} + \cancel{RTH0 \cdot P_{diss2}}$
$RTH0 = (T1_{ambient} - T2_{ambient})/P_{diss1}$



Plot ASM_HEMT_MODELING/DC_RTH_MODELING/idvd_Output_25C/id_vd_T

Id

100, 125, 150 and 175C



Plot ASM_HEMT_MODELING/DC_RTH_MODELING/idvd_Output_25C/rth_extraction

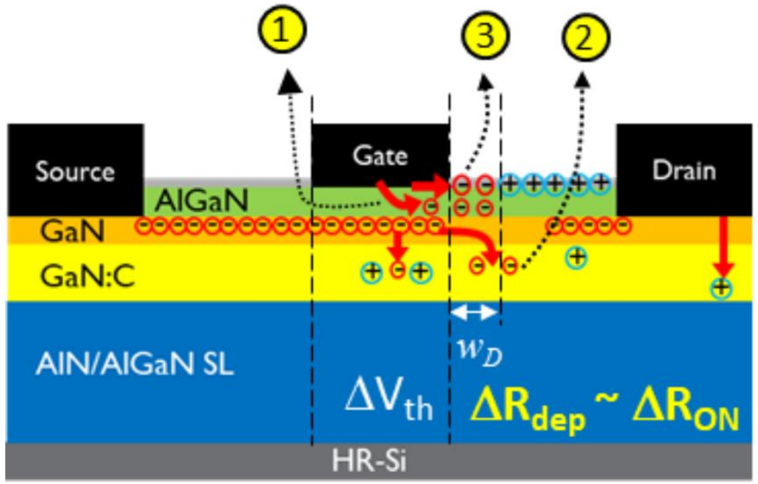
Slope=22K/w

Temp (in Kelvin)

Power

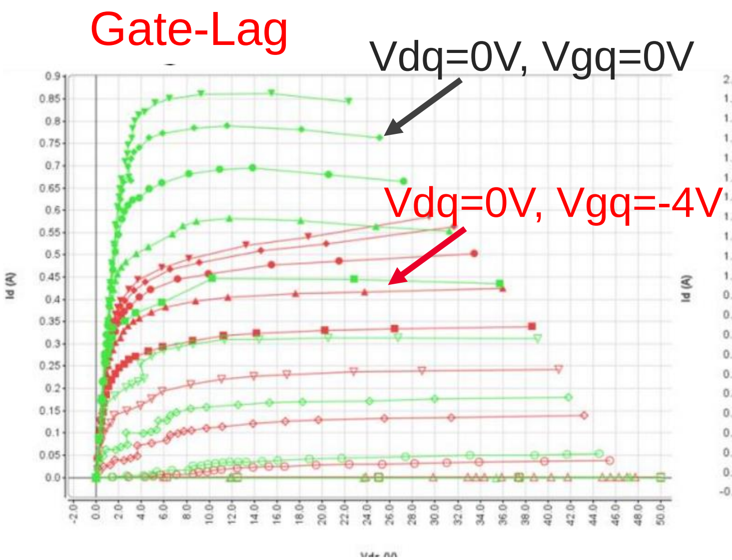
Trapping Effect

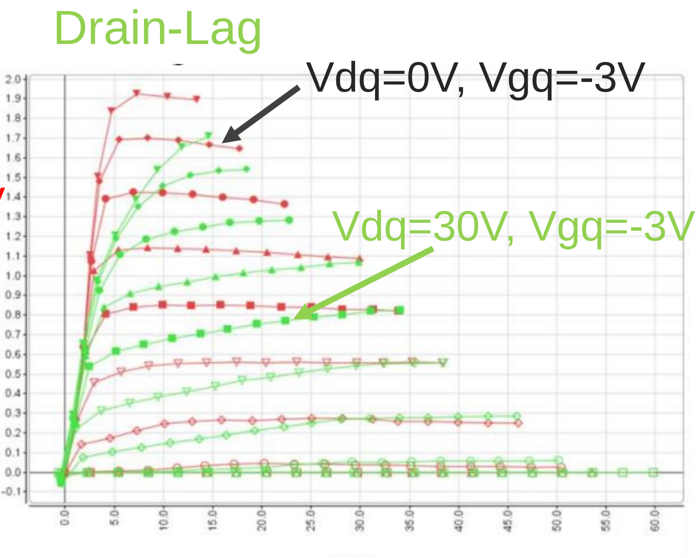
Introduction of Trapping Effect



Charge trapping in the buffer layer and AlGaN/GaN interface layer cause a reduction in 2DEG channel charge density, causing a modulation of drain current I_D.

The trap model accurately captures Dynamic-R_{ON} and knee walkout.





Gate-lag

- **Vdq = 0V**
- **Vgq = Deep OFF condition:**

A strong field through the AlGaN layer. No field through buffer (since Vds = 0). Only surface traps activated.

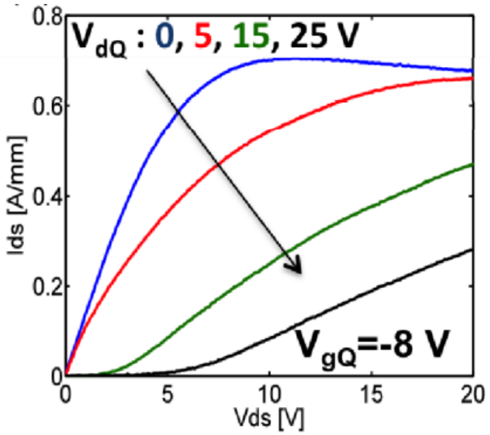
Drain-lag

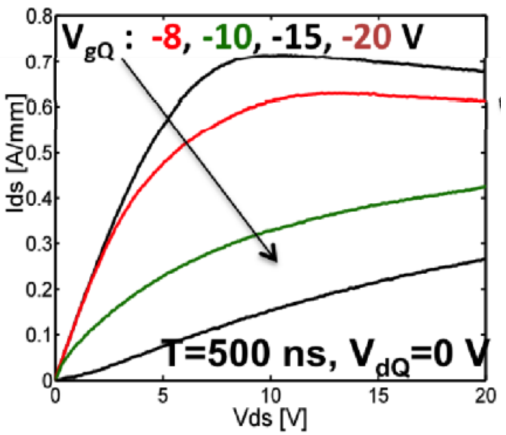
- **Vdq = A significantly positive voltage**
- **Vgq = Deep OFF condition:**

A strong field through the AlGaN layer as well as the buffer. Both surface and buffer traps activated.

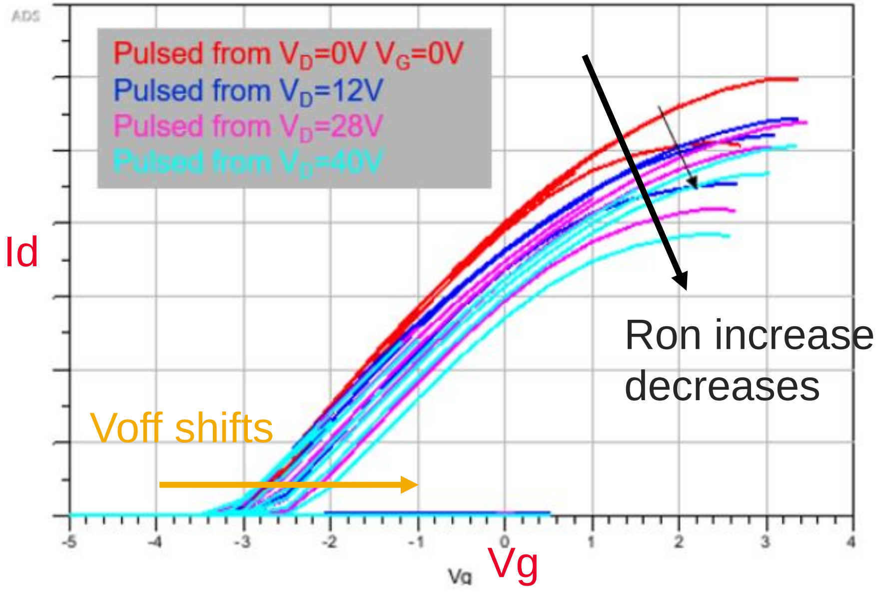
Source: R. Fang, D. Ma, U. Radhakrishna, and L. Wei, "MVSG GaN-HEMT Model: Approach to Simulate Fringing Field Capacitances, Gate Current De-biasing, and Charge Trapping Effects," accepted by *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium*

Pulsed IV Measurements





- Decrease of Ion, increase of Ron and Vdsat
- After voltage stress is removed, a non-negligible time is required for the 2DEG to regain charge.
- Critical for circuit dynamic operations for RF.



Id

Voff shifts

Vg

Ron increases, Ion decreases

- Increase of Ron and cut-off voltage

Source: U. Radhakrishna, D. Piedra, Y. Zhang, T. Palacios and D. Antoniadis, "High voltage GaN HEMT compact model: Experimental verification, field plate optimization and charge trapping," 2013 IEEE International Electron Devices Meeting, Washington,

U. Radhakrishna and L. Wei, “MIT virtual source GaN HEMT: MVSG model manual,” May 1 2022

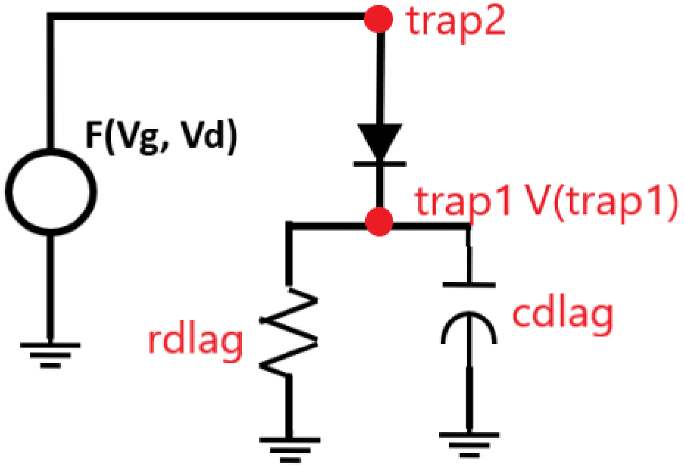
Trapping Extraction

ASM-HEMT Trapping Model 1 and 2

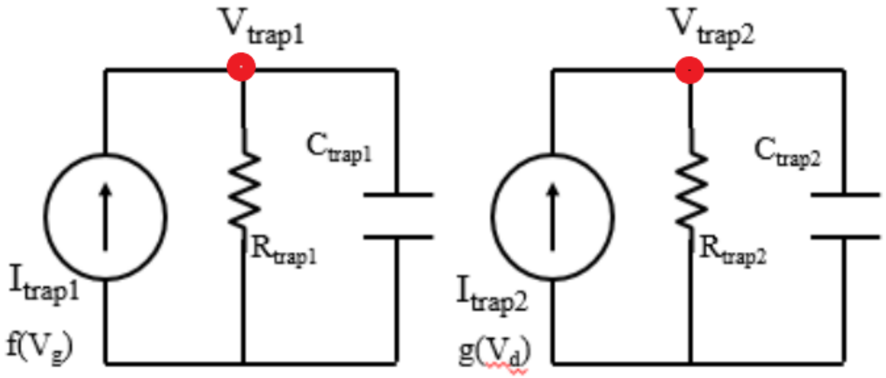
- TRAPMOD=0

  Trapping model turns off
- TRAPMOD=1
  - A single RC sub-circuit
  - Trap voltage V(trap1) will feed back into model
  - voff_cap, eta0_cap, rs_cap, rd_cap changing due to the trapping
- TRAPMOD=2
  - Two RC sub-circuits are used
  - Vtrap1 and Vtrap2 will feed back into model
  - Voff_trap, ron_trap, cdscd_trap, eta0_trap changing due to the trapping

TRAPMOD=1



TRAPMOD=2



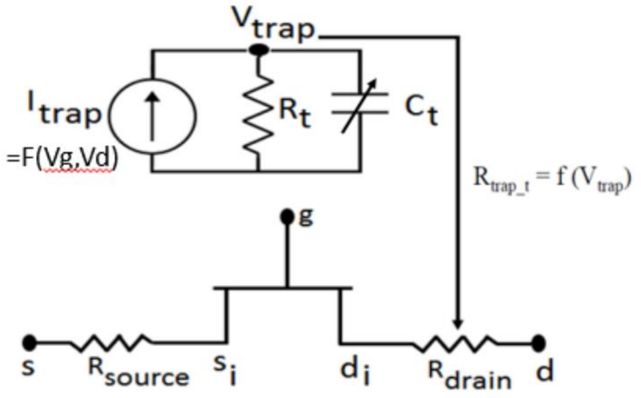
Source: S. Khandelwal, J. Hodges, and N. Reddy, ASM-HEMT 101.3.0 Advanced SPICE Model for HEMTs Technical Manual, Macquarie University

Trapping Extraction

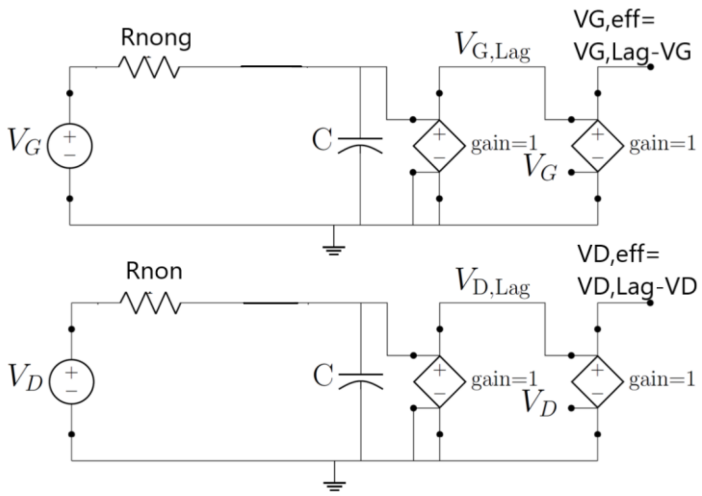
ASM-HEMT Trapping Model 3 and 4

- TRAPMOD=3
  - Single RC sub-circuit
  - Recommended for GaN power device dynamic ON-resistance
  - Only **drain-side resistance** is affected
- **TRAPMOD=4**
  - Two RC sub-circuits are used
  - Model drain-lag and gate-lag with most flexibility
  - **voffglag, u0glag, vsatglag** changing due to gate-lag ($V_{G,eff}$)
  - **voffdlag, ns0sdlag, ns0ddlag** changing due to drain-lag ($V_{D,eff}$)

TRAPMOD=3



TRAPMOD=4



Trapping Extraction

MVSG_CMC Charge Trapping Model

- TRAPSELECT=0

  Trapping model turns off

- TRAPSELECT=1

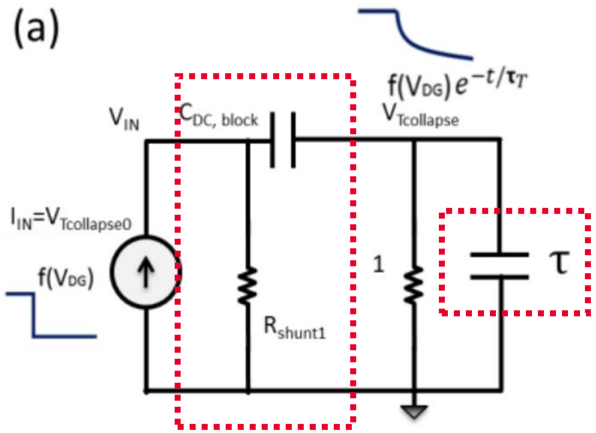
  A single RC network with a constant time τ is used for modeling trapping and de-trapping constant time.

- **TRAPSELECT=2 (new)**

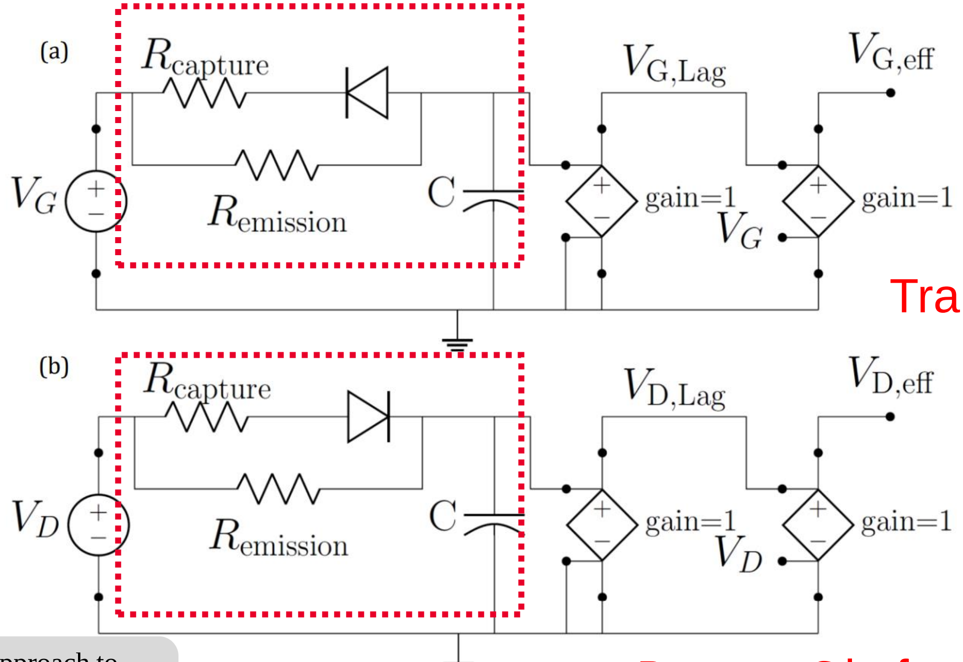
  Two parallel R-branches in an RC network with an ideal series diode on one of the resistance branches.

  Two-time constants are used.

  Recommended due to more flexibility



Trapping model 1



Trapping model 2

$\tau_{capture} \approx R_{capture}C$ in forward-biased

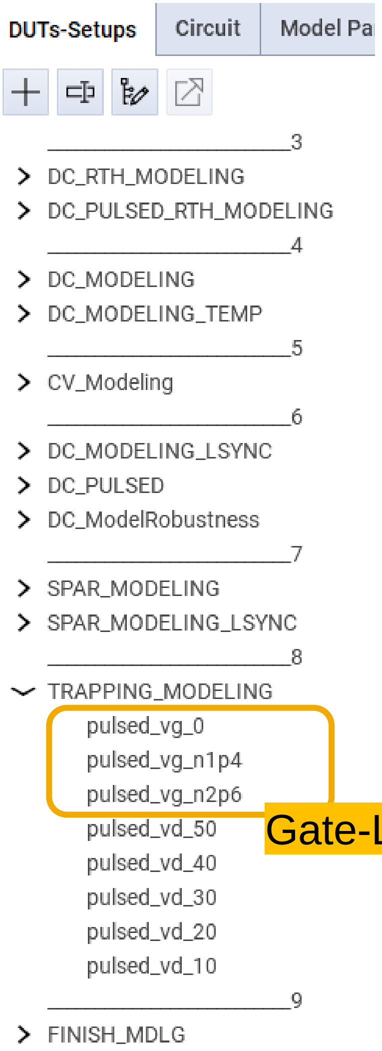
$\tau_{emission} \approx R_{emission}C$ in reverse-biased

Source: R. Fang, D. Ma, U. Radhakrishna, and L. Wei, "MVSG GaN-HEMT Model: Approach to Simulate Fringing Field Capacitances, Gate Current De-biasing, and Charge Trapping Effects," accepted by *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium*

Trapping Extraction (ASM-HEMT)

Gate Lag Trapping Extraction

Extraction flow



3
- DC_RTH_MODELING
- DC_PULSED_RTH_MODELING

4
- DC_MODELING
- DC_MODELING_TEMP

5
- CV_Modeling

6
- DC_MODELING_LSYNC
- DC_PULSED
- DC_ModelRobustness

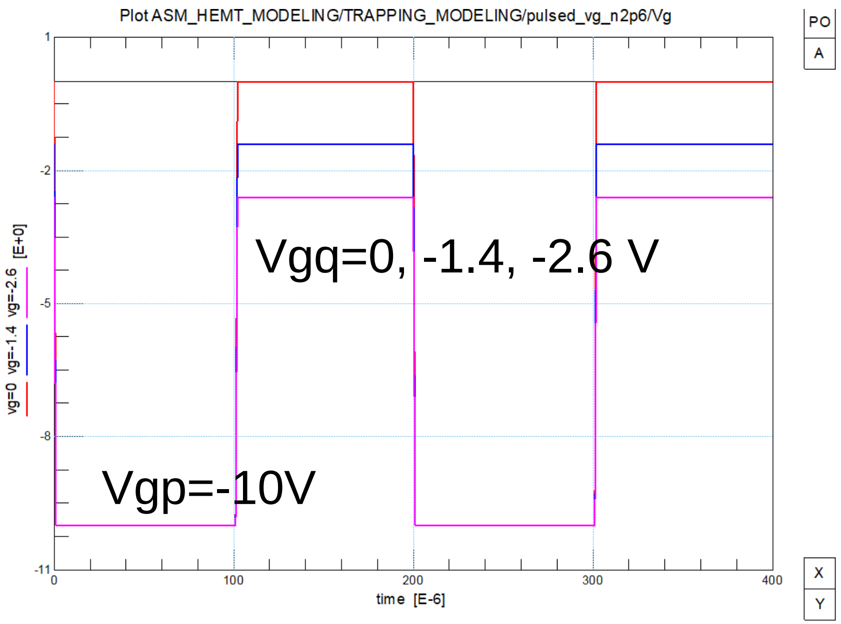
7
- SPAR_MODELING
- SPAR_MODELING_LSYNC

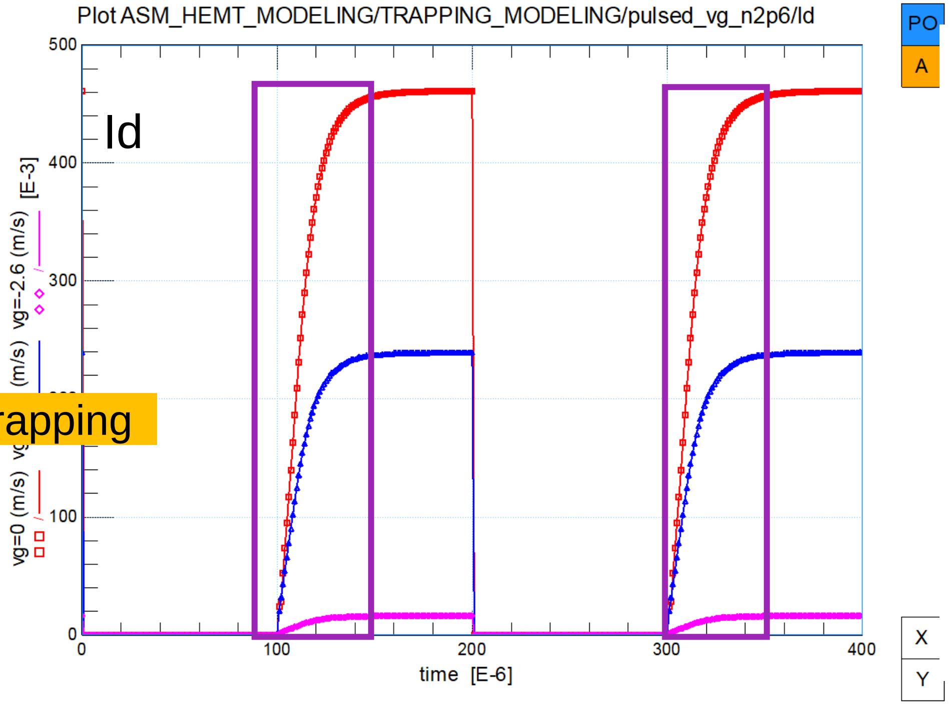
8
- TRAPPING_MODELING
  - pulsed_vg_0
  - pulsed_vg_n1p4
  - pulsed_vg_n2p6
  - pulsed_vd_50
  - pulsed_vd_40
  - pulsed_vd_30
  - pulsed_vd_20
  - pulsed_vd_10

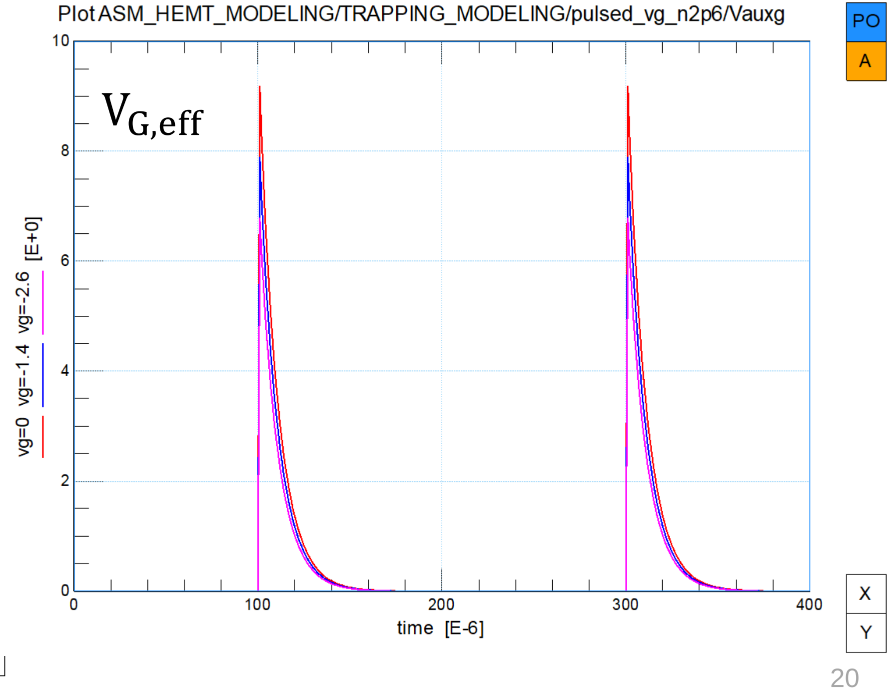
9
- FINISH_MDLG

Gate-Lag trapping

- TRAPMOD=4 is used
- Gate-lag-related parameters can be tuned.
- **voffglag, u0glag, vsatglag** related trapping parameters



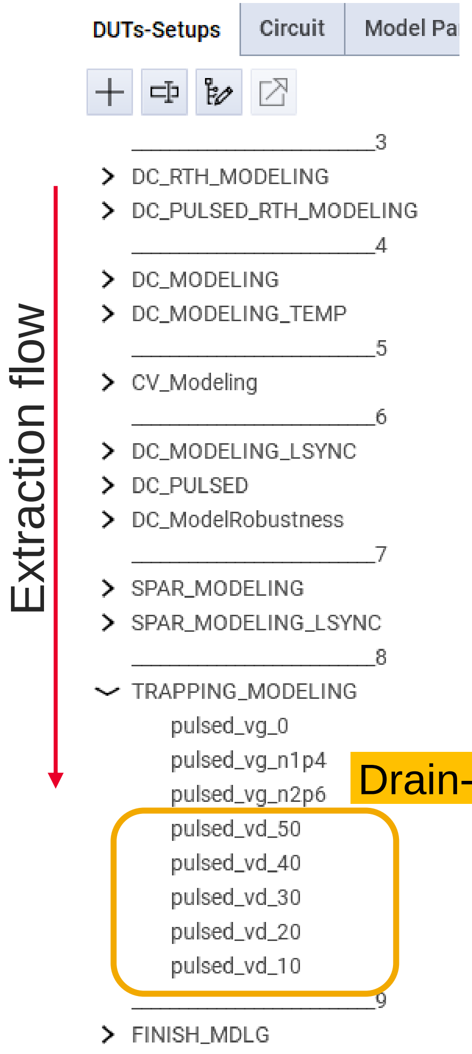




KEYSIGHT

Trapping Extraction (ASM-HEMT)

Drain Lag Trapping Extraction



Extraction flow

DUTs-Setups | Circuit | Model Pa

3
- DC_RTH_MODELING
- DC_PULSED_RTH_MODELING

4
- DC_MODELING
- DC_MODELING_TEMP

5
- CV_Modeling

6
- DC_MODELING_LSYNC
- DC_PULSED
- DC_ModelRobustness

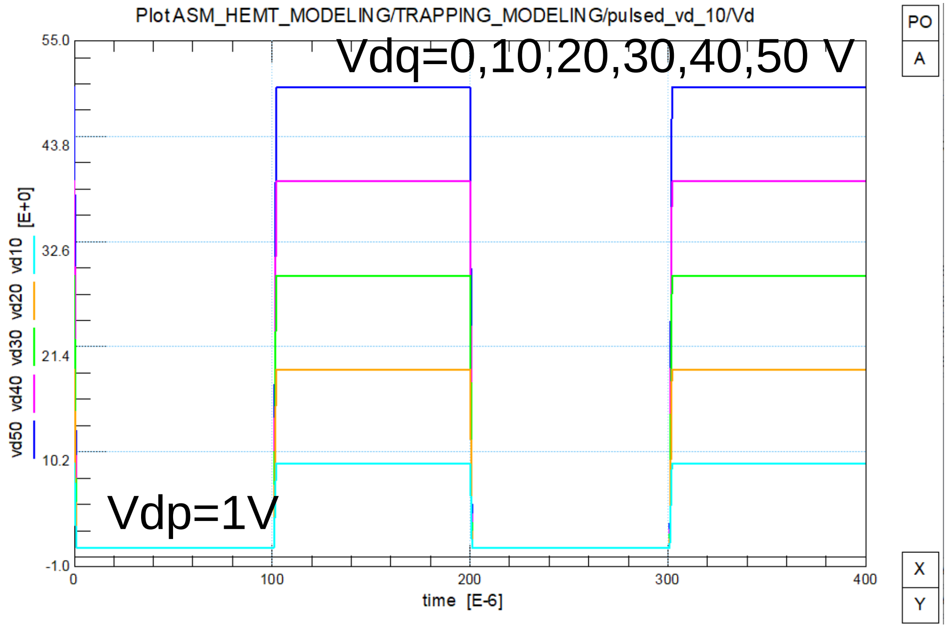
7
- SPAR_MODELING
- SPAR_MODELING_LSYNC

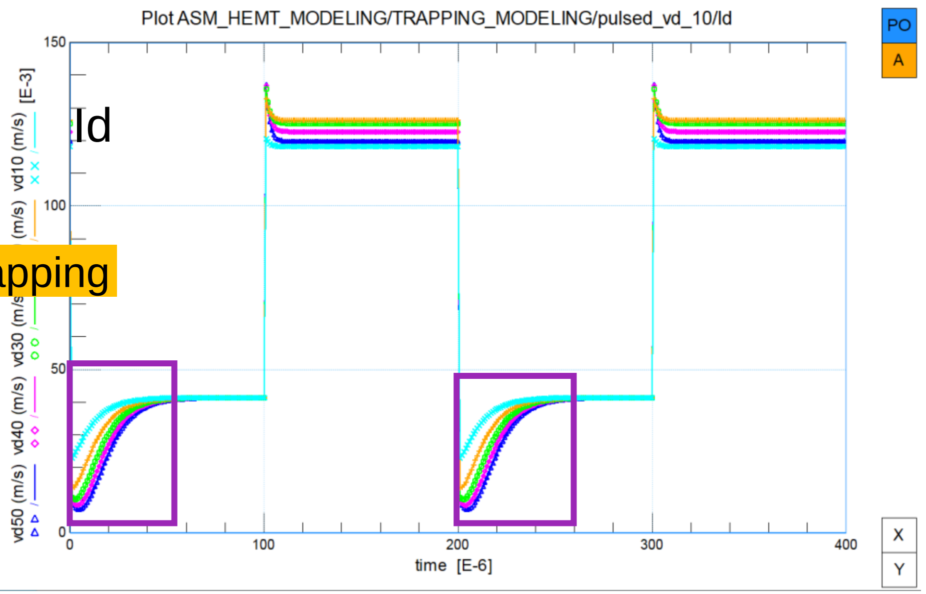
8
- TRAPPING_MODELING
  - pulsed_vg_0
  - pulsed_vg_n1p4
  - pulsed_vg_n2p6
  - pulsed_vd_50
  - pulsed_vd_40
  - pulsed_vd_30
  - pulsed_vd_20
  - pulsed_vd_10

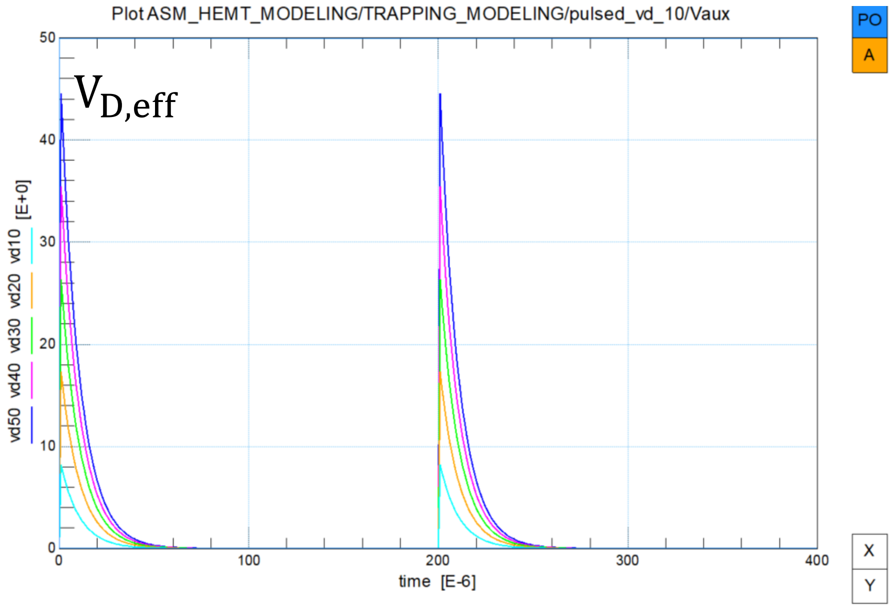
9
- FINISH_MDLG

Drain-Lag trapping

- TRAPMOD=4 is used
- Drain-lag-related parameters can be tuned.
- **voffdlag, ns0sdlag, ns0ddlag** related trapping parameters







Summary

- The latest version of ASM-HEMT 101.4 and MVSG_CMC 3.2.0 is implemented in ADS 2024 update 1
- The RF package with ASM-HEMT 101.3 and MVSG_CMC 3.1.0 is implemented in IC-CAP 2023 and newer version
- Both ASM-HEMT and MVSG_CMC have good performance on GaN HEMTs modeling:
  - Core model for DC
  - CV and S-parameters
  - Thermal extraction – implemented in both ASM-HEMT and MVSG_CMC parameter flow
  - Trapping extraction – implemented in MVSG_CMC parameter flow

    will implement in ASM-HEMT parameter flow soon

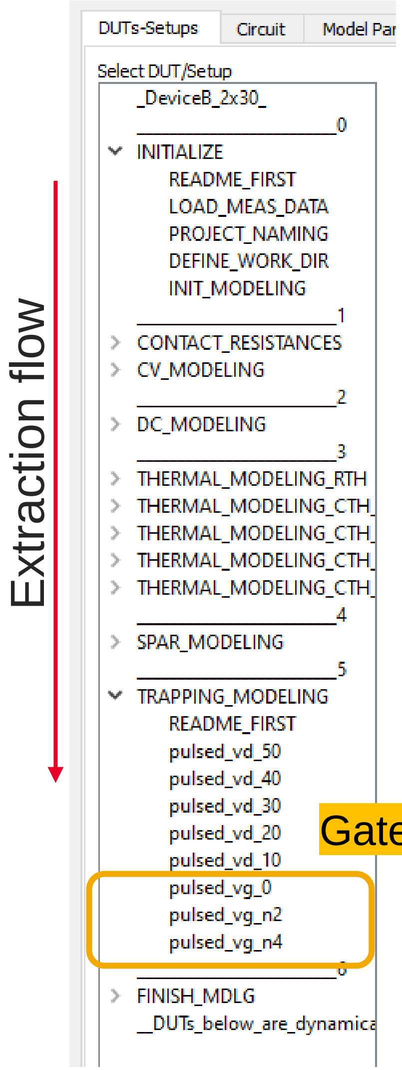
Thanks

- Thanks to Prof. Sourabh Khandelwal, developer of ASM-HEMT, for his help in the development of ASM-HEMT parameter flow in IC-CAP
- Thanks to Prof. Lan Wei, developer of MVSG_CMC, for her help in the development of MVSG_CMC parameter flow in IC-CAP

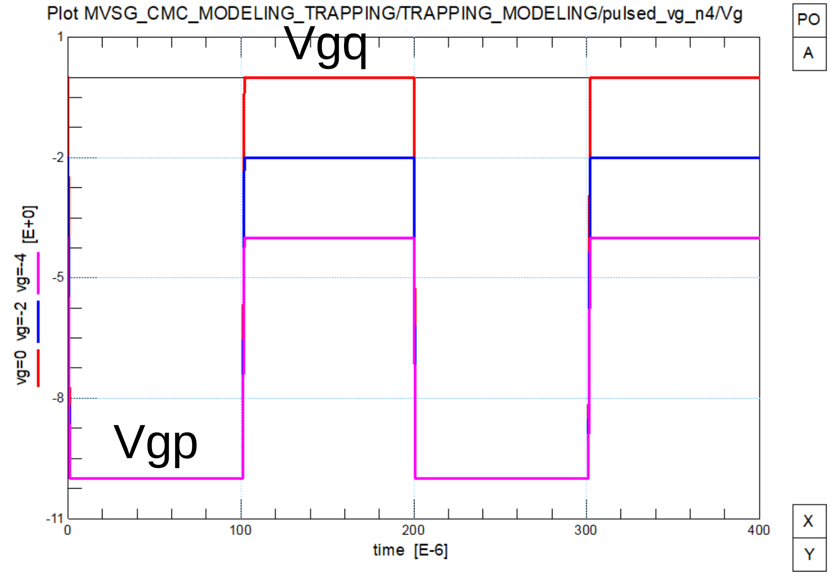
Thank you

Trapping Extraction

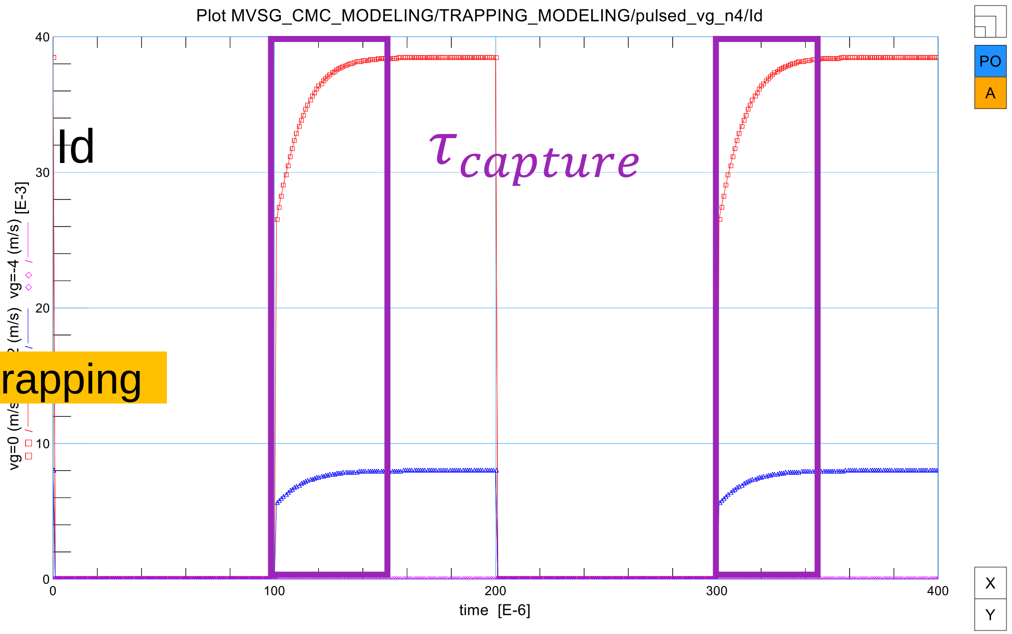
Gate Lag Trapping Extraction

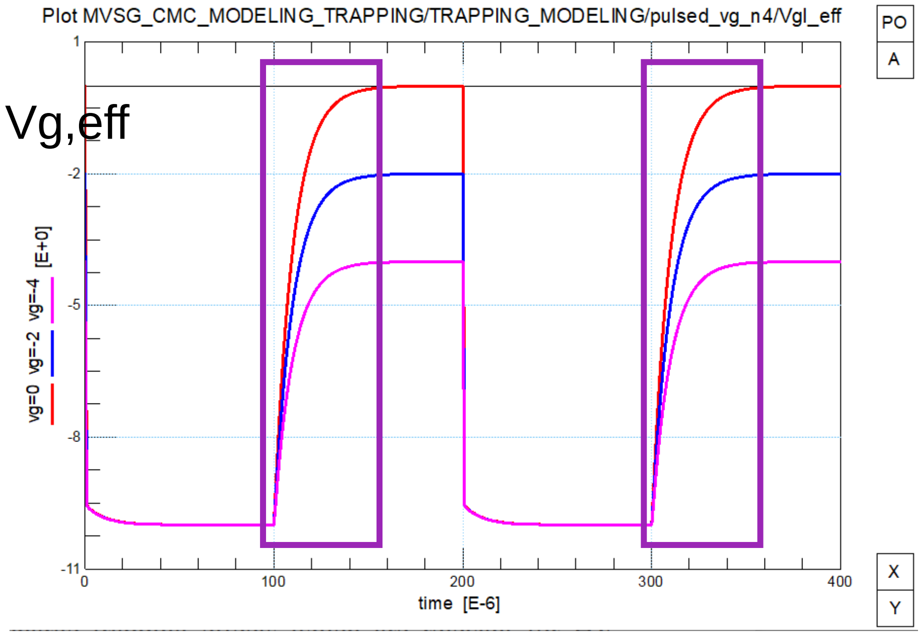


- We select new trapping model with TRAPSELECT=2
- Mainly parameters can be used: rcapture=rslow, remission=rfast, vdltrapth



Gate-Lag trapping

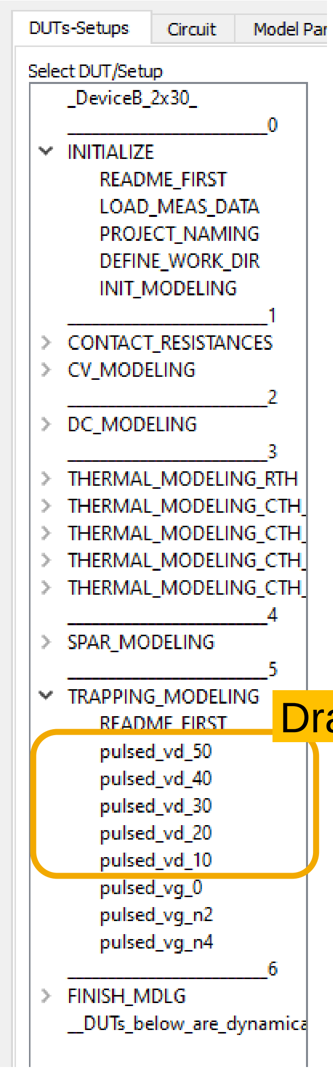




Trapping Extraction

Drain Lag Trapping Extraction

Extraction flow



DUTs-Setups | Circuit | Model Par

Select DUT/Setup

- _DeviceB_2x30_
- ________________0
- INITIALIZE
  - README_FIRST
  - LOAD_MEAS_DATA
  - PROJECT_NAMING
  - DEFINE_WORK_DIR
  - INIT_MODELING
- ________________1
- CONTACT_RESISTANCES
- CV_MODELING
- ________________2
- DC_MODELING
- ________________3
- THERMAL_MODELING_RTH
- THERMAL_MODELING_CTH_
- THERMAL_MODELING_CTH_
- THERMAL_MODELING_CTH_
- THERMAL_MODELING_CTH_
- ________________4
- SPAR_MODELING
- ________________5
- TRAPPING_MODELING
  - README_FIRST
  - pulsed_vd_50
  - pulsed_vd_40
  - pulsed_vd_30
  - pulsed_vd_20
  - pulsed_vd_10
  - pulsed_vg_0
  - pulsed_vg_n2
  - pulsed_vg_n4
- ________________6
- FINISH_MDLG
- __DUTs_below_are_dynamica

Drain-Lag trapping

- We select new trapping model with TRAPSELECT=2
- Mainly parameters can be used: rcapture=rslow, remission=rfast, vgltrapth