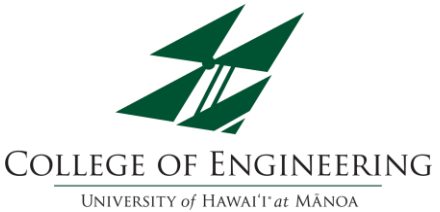
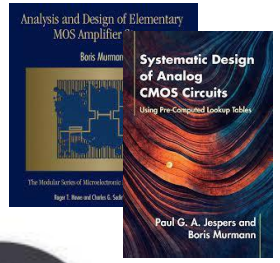
Re-Energizing Analog Design using the Open-Source Ecosystem

Boris Murmann
bmurmann@hawaii.edu
December 13, 2023

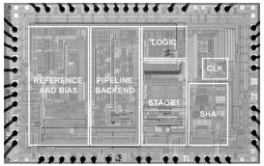


My Journey



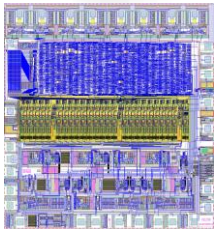
20 years of teaching & consulting

2003
PhD chip
0.35µm CMOS



1980s
PCB design

IC design is not cool anymore?



1994
First chip
2µm CMOS

If you need short-term gratification, don't be a chip designer!

20/03/18

Daniel Saddi Associate Director

SIGN IN The Register®

{* SYSTEMS *}

America's chip land has another potential shortage: Electronics engineers

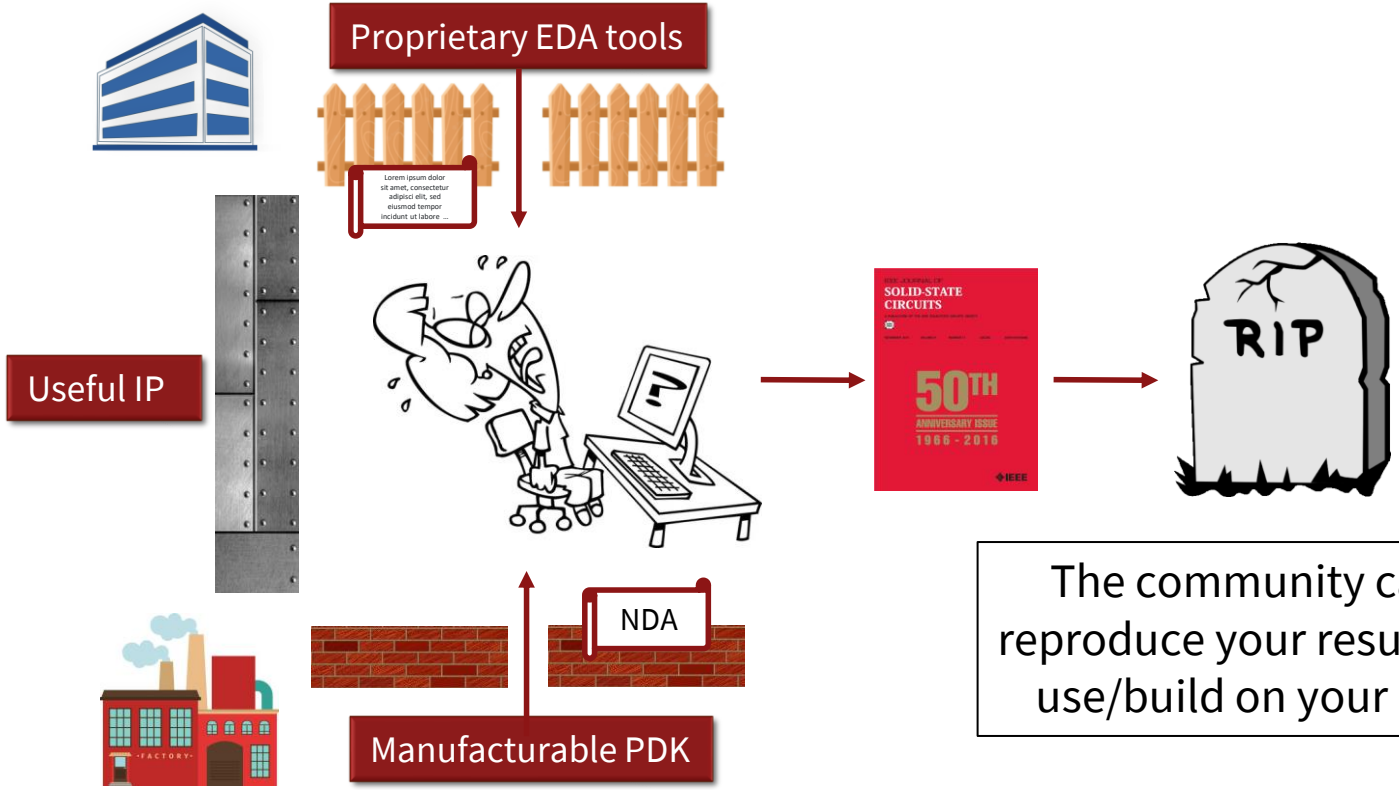
Why screw around writing Verilog when you can earn tons more with Python, Java or Go?

Dylan Martin

Fri 8 Jul 2022 // 18:28 UTC

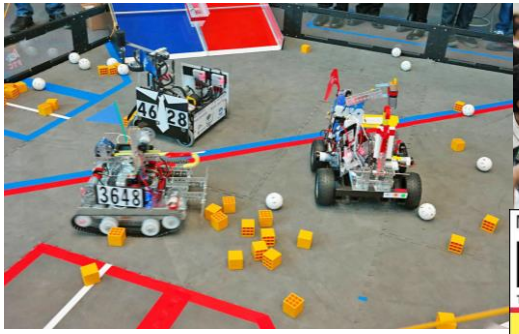
51

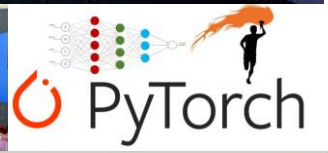
IC Researcher's Perspective

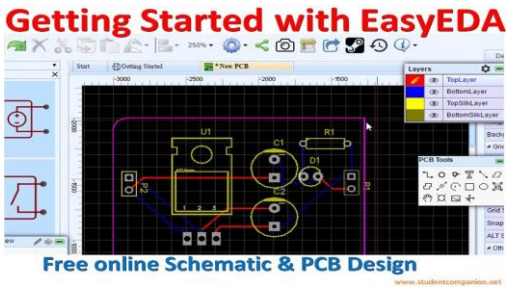


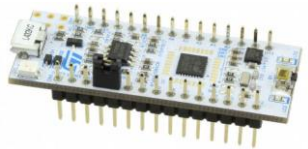
The community cannot reproduce your results or re-use/build on your design

This is Very Different in Other Fields!

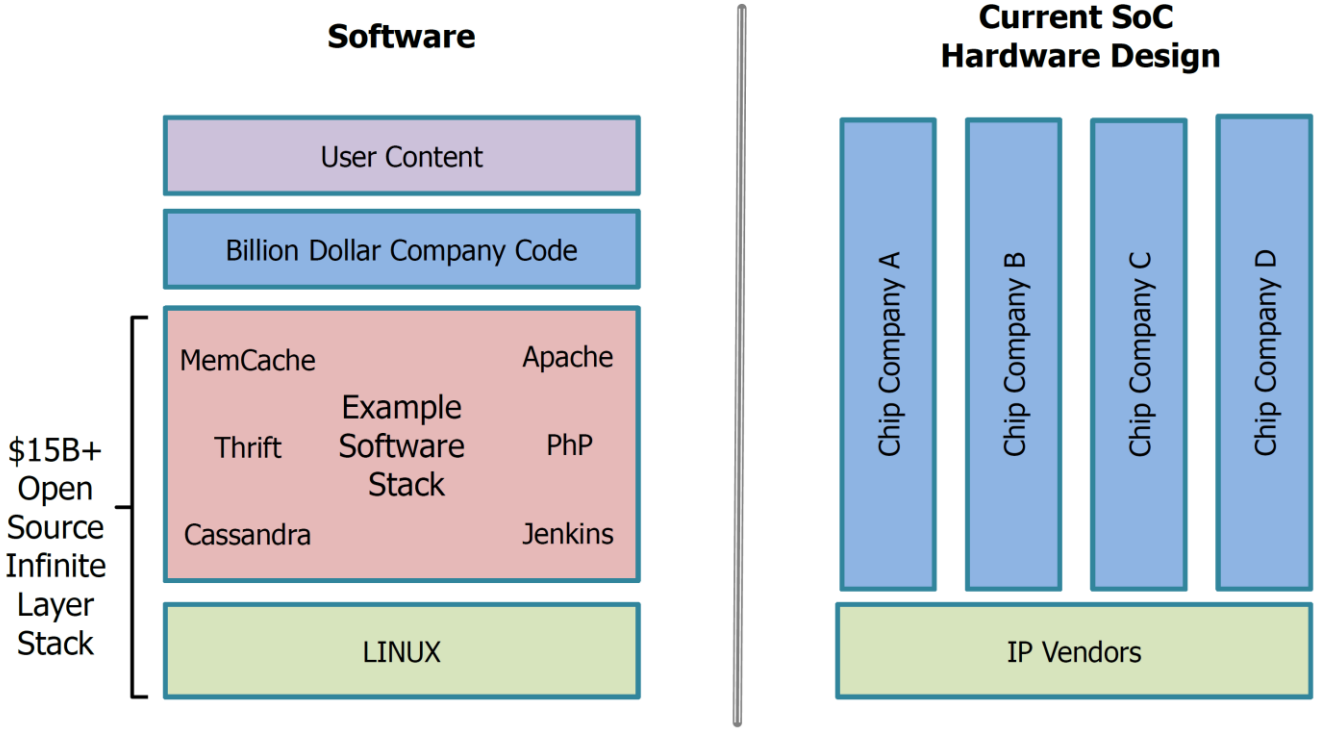




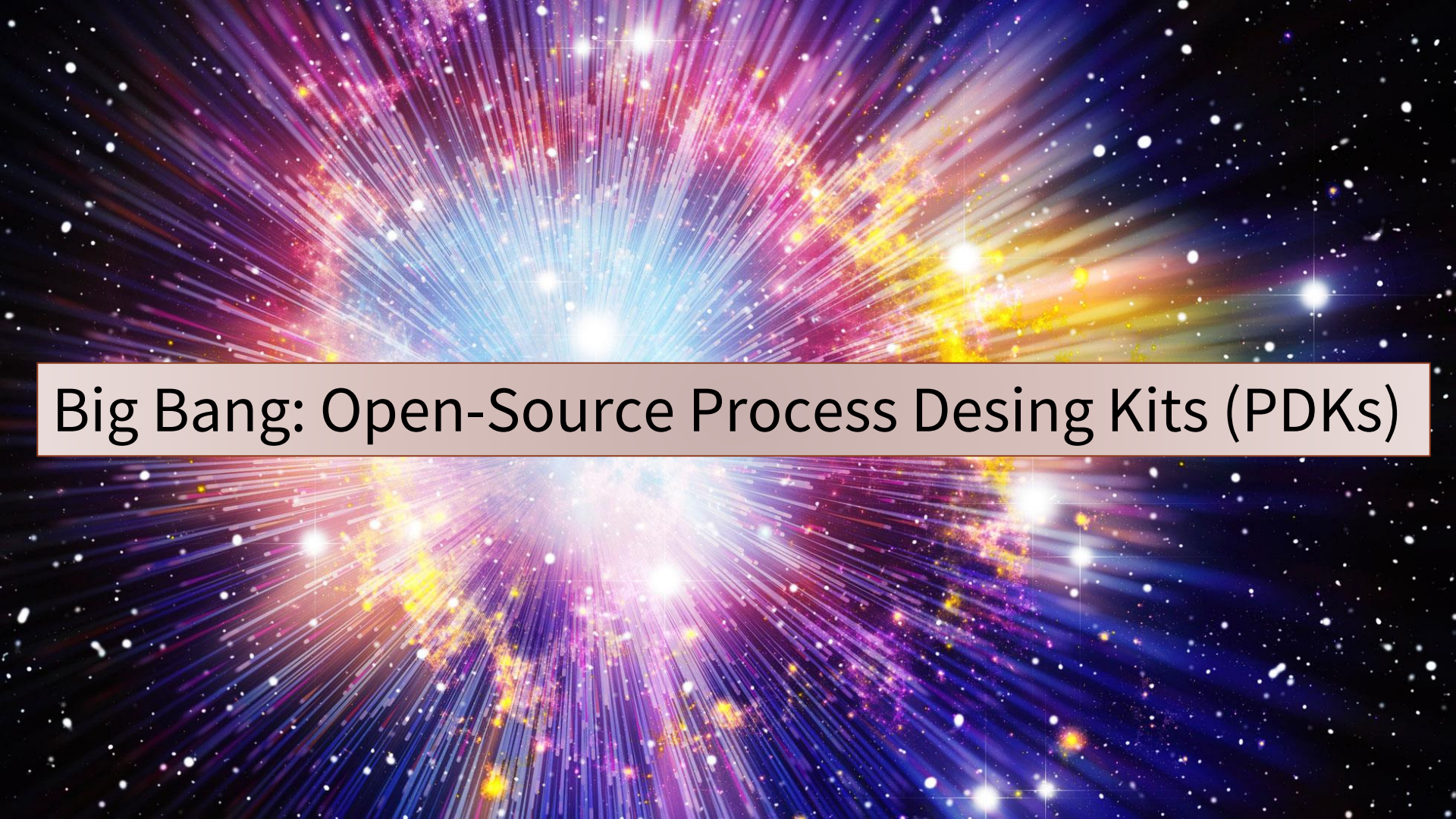




Industry Perspective: Deep Silos, Long Cycles



Source: Andreas Olofsson (DARPA)


Big Bang: Open-Source Process Desing Kits (PDKs)

Open-Source PDKs

- First open-source PDK (November 2020)
  - SkyWater 130nm CMOS
  - https://github.com/google/skywater-pdk
- Second open-source PDK (October 2022)
  - GlobalFoundries 180nm MCU
  - https://github.com/google/gf180mcu-pdk
- Third open-source PDK (March 2023)
  - IHP 130nm BiCMOS
  - https://github.com/IHP-GmbH/IHP-Open-PDK
- Permissive Apache 2.0 licensing

Tim (mithro) Ansell (They/Them) · 1st
Software Engineer at Google

Google + skywater TECHNOLOGY + ihp + GLOBAL FOUNDRIES

Open Source in a Nutshell

- Core principles
  - Open exchange, collaboration, transparency, meritocracy
- Typical benefits (as seen in the software community)
  - Improves productivity, managing complexity
  - Enables community review and steady improvements, re-use
  - Promotes education and tinkering
- Open source does not imply “free”
  - Can make money with open-source products (Red Hat, Ruby on Rails, …)
  - Proper terminology
    - Proprietary vs. open source (NOT: commercial vs. open source)

1. Honeymoon phase
2. What’s next?

Google-Sponsored (Free) Shuttle Runs

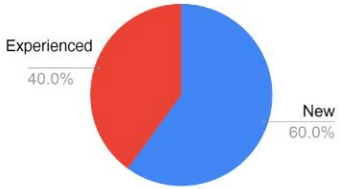
efabless.com

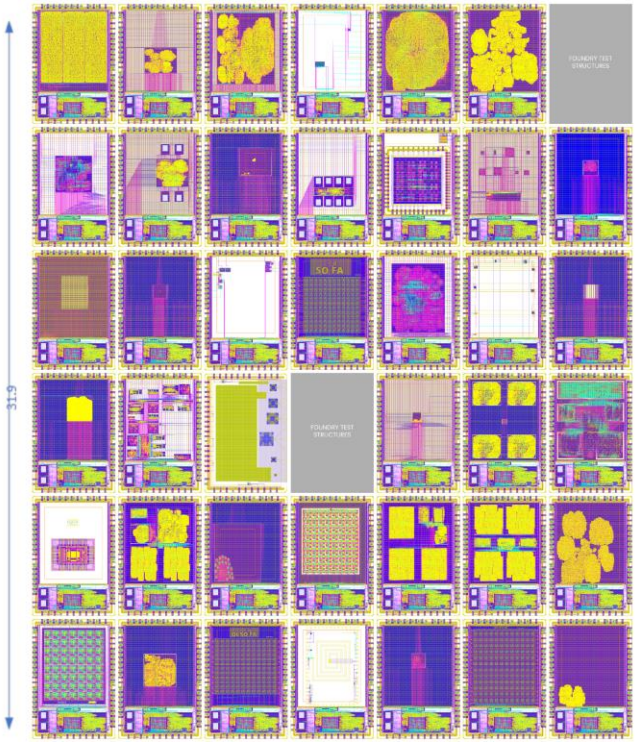
GOOGLE's MPW-ONE

First MPW Overbooked 45/40

45 designs submitted
in **30 days!**

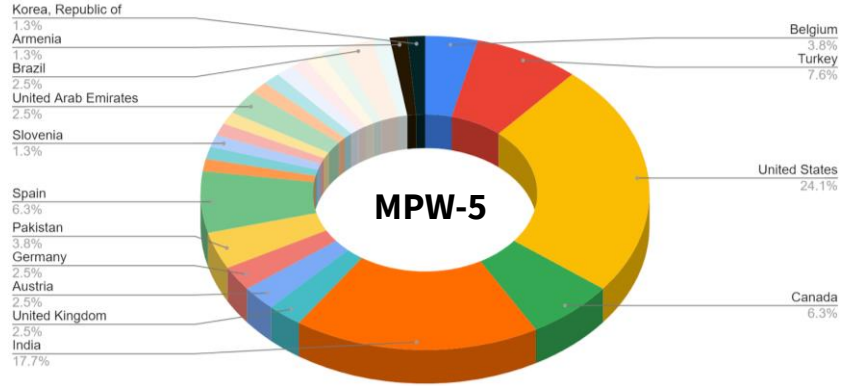
60% by first time designers!

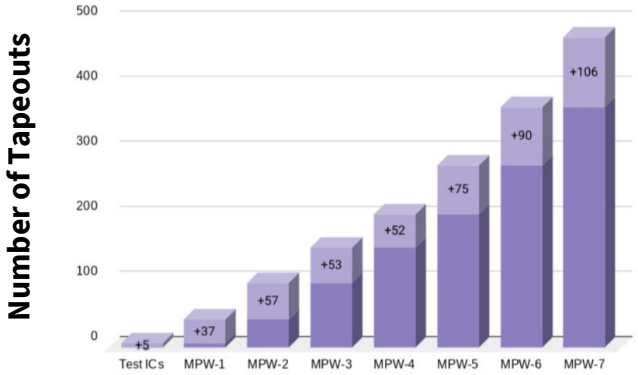




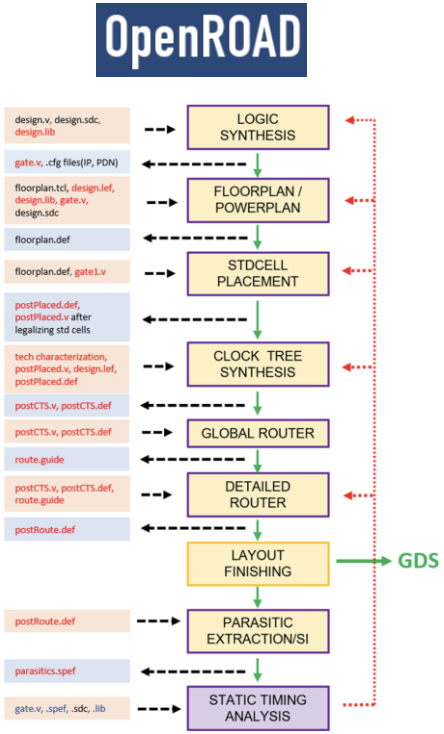
Strong Community Growth

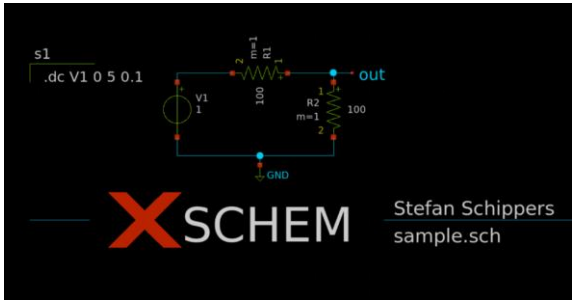
Efabless Caravel “Harness” SoC





Open-Source EDA Tools





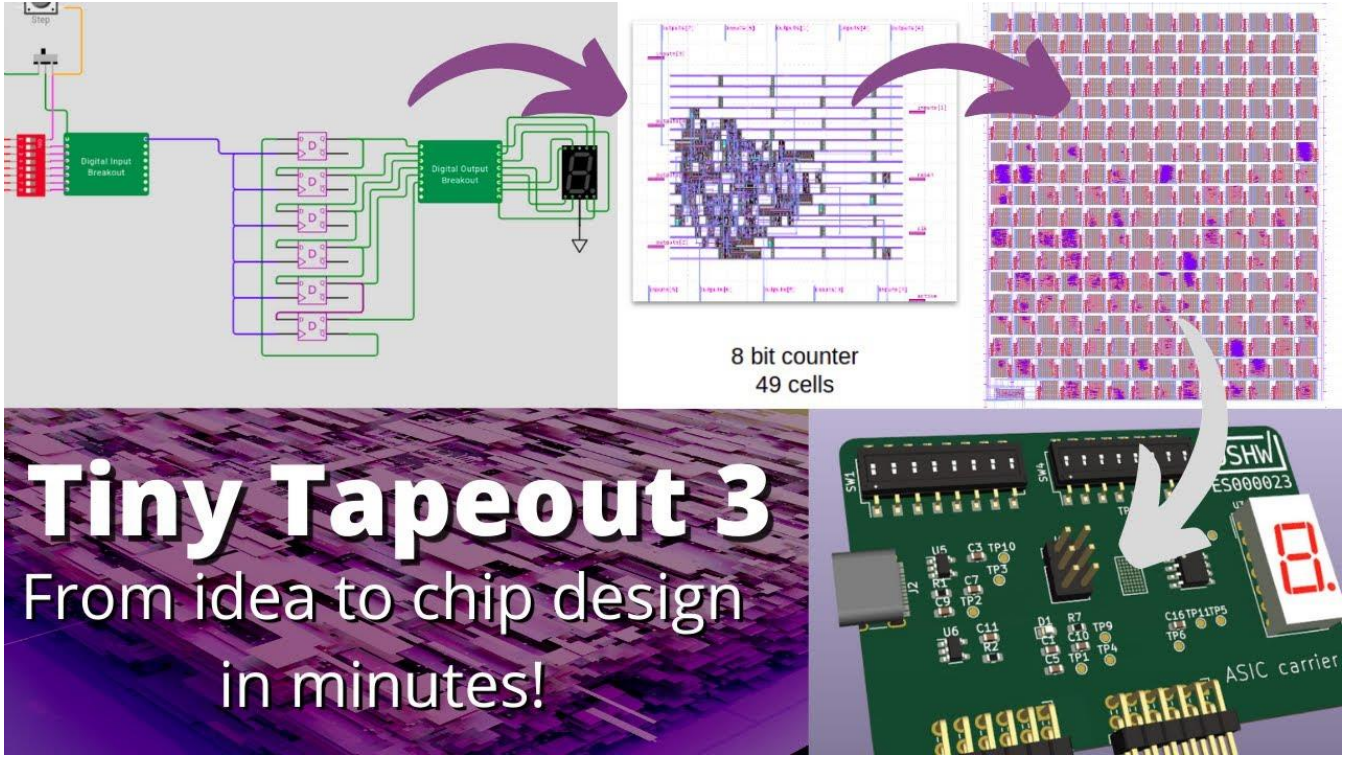
KLayout

NGSPICE

Sandia National Laboratories Xyce
Parallel electronic simulation

GDS_FACTORY

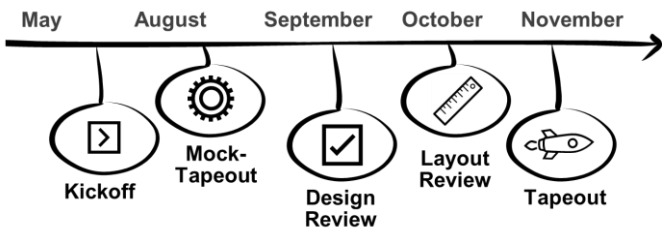
Tiny Tapeouts!

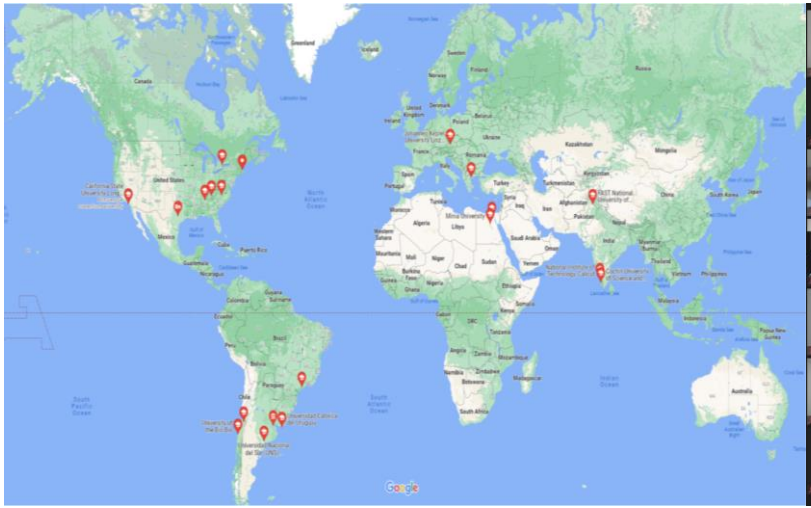


Matt Venn

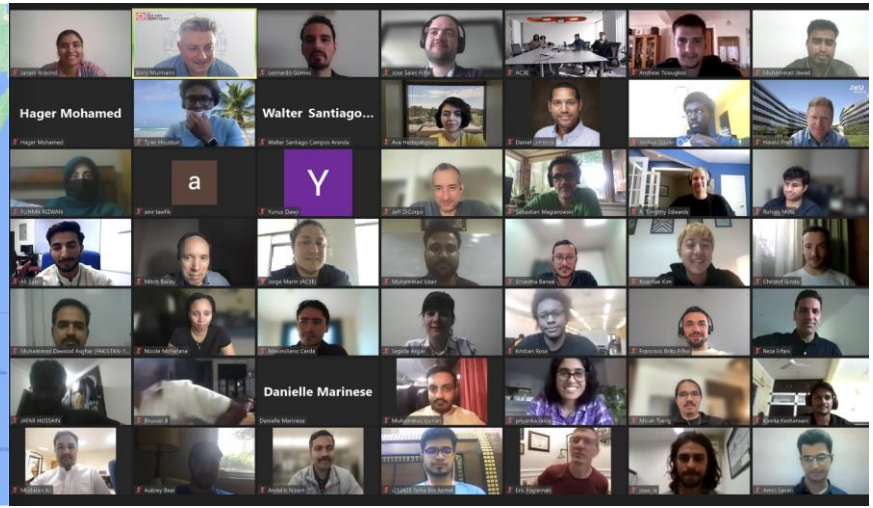
SSCS PICO Chipathon

- 2021: 61 submissions, 18 selected (11 taped out)
- 2022: 54 submissions, 22 selected (14 taped out)



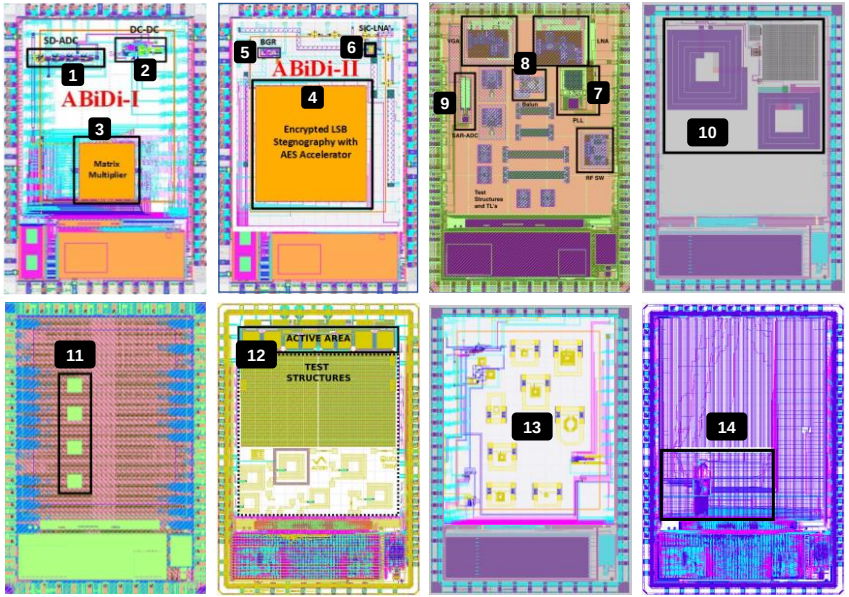


2022 selected teams from 10 countries, 5 continents



June 22, 2022, kick-off meetup with over 100 attendees

2022 Chipathon



	Function	Team	Chip URL
1	Spatial Sigma-Delta ADC	Pakistan1 (FAST National University)	https://platform.efabless.com/projects/1486
2	On-Chip DCDC Converter with Fast Transient Response	Pakistan4 (FAST National University)	
3	Matrix Multiplier for AI at the Edge	Pakistan7 (FAST National University)	
4	Encrypted LSB Steganography with AES Accelerator	Pakistan2 (FAST National University)	https://platform.efabless.com/projects/1443
5	CMOS Bandgap Reference	Pakistan3 (FAST National University)	
6	Self-Interference Cancellation LNA	Pakistan4 (FAST National University)	
7	Sub-Sampling PLL for SerDes Applications	Austria (Johannes Kepler Univ., Linz)	https://platform.efabless.com/projects/1431
8	60 GHz Demonstrator Chip	Brazil (University of São Paulo)	
9	Low-Power 10-bit SAR ADC	USA1 (University of Alabama & MIT Lincoln Lab)	
10	Boost Converter for Battery-Powered IoT Applications	Greece (Aristotle University of Thessaloniki)	https://platform.efabless.com/projects/1457
11	Radiation-Hardened ALU	USA2 (North Carolina A&T State University)	https://platform.efabless.com/projects/1593
12	DC-DC Buck Converter for CubeSat	Chile[1]/Argentina[2]/Uruguay[3] [1]Universidad Técnica Fed. Santa María [2]Universidad Nacional del Sur & Instituto Nacional de Tecnología Industrial [3]Universidad Católica	https://platform.efabless.com/projects/1427
13	Electrochemical Water Quality Monitoring	USA5 (University of Tennessee)	https://platform.efabless.com/projects/1469
14	Mix-Pix - A Mixed-Signal Circuit for Smart Imaging	Chile (Universidad del Bío-Bío)	https://platform.efabless.com/projects/1494

Magazine article: “Meet the SSCS PICO Chipathletes,” https://ieeexplore.ieee.org/document/9950763

Team Diversity

Chile/Argentina/Uruguay

Egypt 2

USA 2

Greece

Pakistan 6

Pakistan 4

"Meet the Chipathletes,"
SSCS Magazine, Fall 2022

CHIPS (Common Hardware for Interfaces, Processors and Systems) Alliance harnesses the energy of open source collaboration to accelerate hardware development.

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IC Innovation

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ISSCC "Code-a-Chip" Travel Grant Awards

ISSCC "Code-a-Chip" Travel Grant Awards

SUBMISSION DEADLINE: NOVEMBER 21, 2022

The ISSCC 2023 Code-a-Chip Travel Grant Award was created to (1) promote reproducible chip design using open-source tools and notebook-driven design flows and (2) enable up-and-coming talents as well as seasoned open source enthusiasts to travel to the Conference and interact with the leading-edge chip design community. This program is made possible by a donation from the CHIPS Alliance, a non-profit organization hosted by The Linux Foundation.

Program rules

- The program is open to anyone (no restrictions). Membership in the IEEE Solid-State Circuits Society (SSCS) membership is encouraged, but not required. Teaming is encouraged, but each team must identify a single leader who can travel to the ISSCC from February 19-23, 2023, to receive the award.
- Applicants must submit an open-source Jupyter notebook detailing an innovative circuit design using open-source tools (examples: inverter, temperature sensor)
- Each submission must contain a suitable open source license (e.g., Apache 2.0).

Made possible by a donation from the CHIPS Alliance

CHIPS ALLIANCE

https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io

Motivation: Reproducible IC Design

- It is common to publish with code in other disciplines
  - Now also possible in IC design!

Get OpenLane

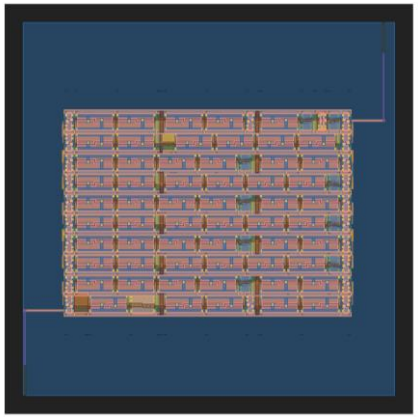
```
$ git clone --depth=1 https://github.com/The-OpenROAD-Project/OpenLane
```

Write verilog

```
%%writefile inverter.v
module inverter(input wire in, output wire out);
    assign out = !in;
endmodule
```

Run OpenLane Flow

```
import os
import pathlib
OPENLANE_ROOT=str(pathlib.Path('OpenLane').resolve())
PATH=os.environ['PATH']
%env PDK_ROOT={CONDA_PREFIX}/share/pdk
%env TCLLIBPATH={CONDA_PREFIX}/lib/tcllib1.20
%env OPENLANE_ROOT={OPENLANE_ROOT}
%env PATH={PATH}:{OPENLANE_ROOT}:{OPENLANE_ROOT}/scripts
%env OPENLANE_LOCAL_INSTALL=1
!flow.tcl -design .
```



https://developers.google.com/silicon/guides/digital-inverter-openlane

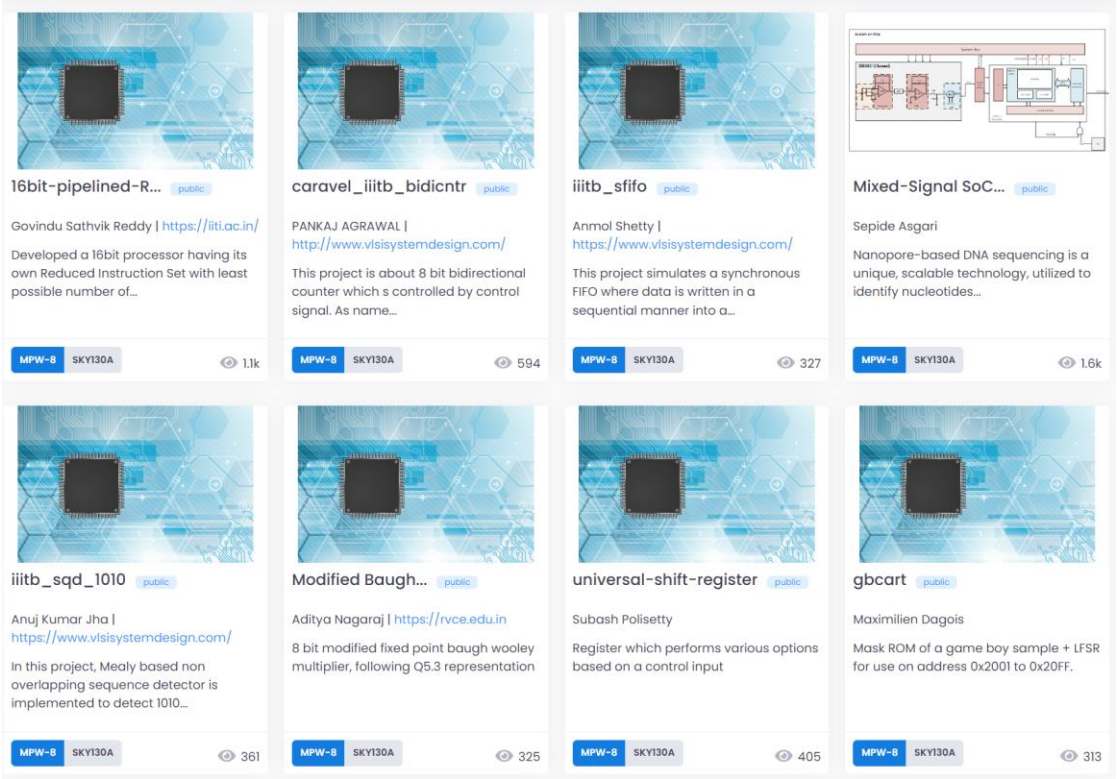
1. Honeymoon phase

2. What’s next?

Challenges & Opportunities – Thigs We Need to Work On…

- Limited functionality of open-source EDA tools
- Maintenance of tools & repos
- Best practices for team collaboration
- Standards for documentation & validation of “IP”
- Leveraging open-source for analog design automation
  - “Grand challenge”

Lots of Repos…



- Can we call these “IP”?
- How to re-use?
- How to trust?
- Still a lot to learn from software community

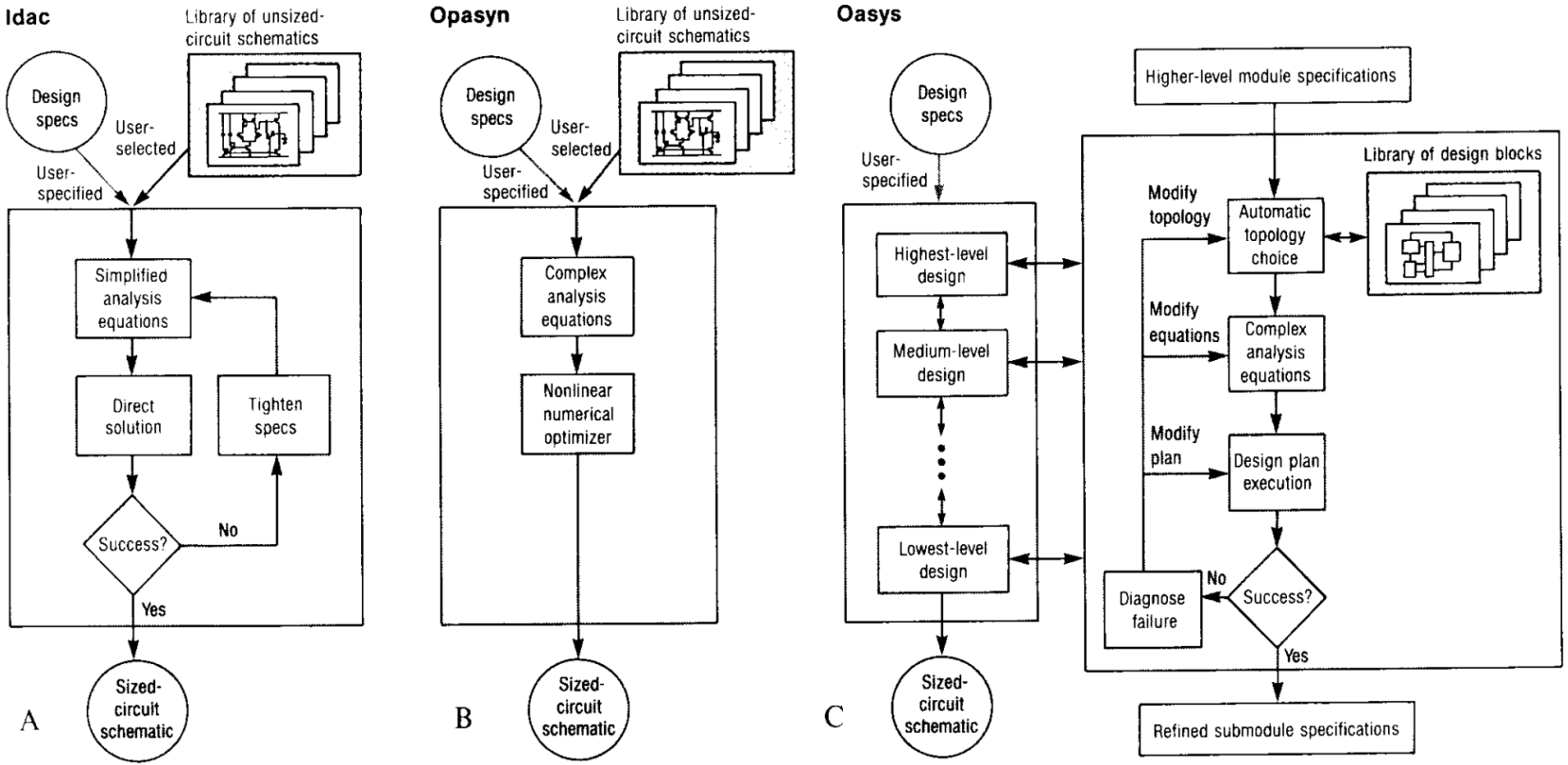
How to automate analog IC designs

L. Richard Carley and Rob A. Rutenbar
Carnegie Mellon University

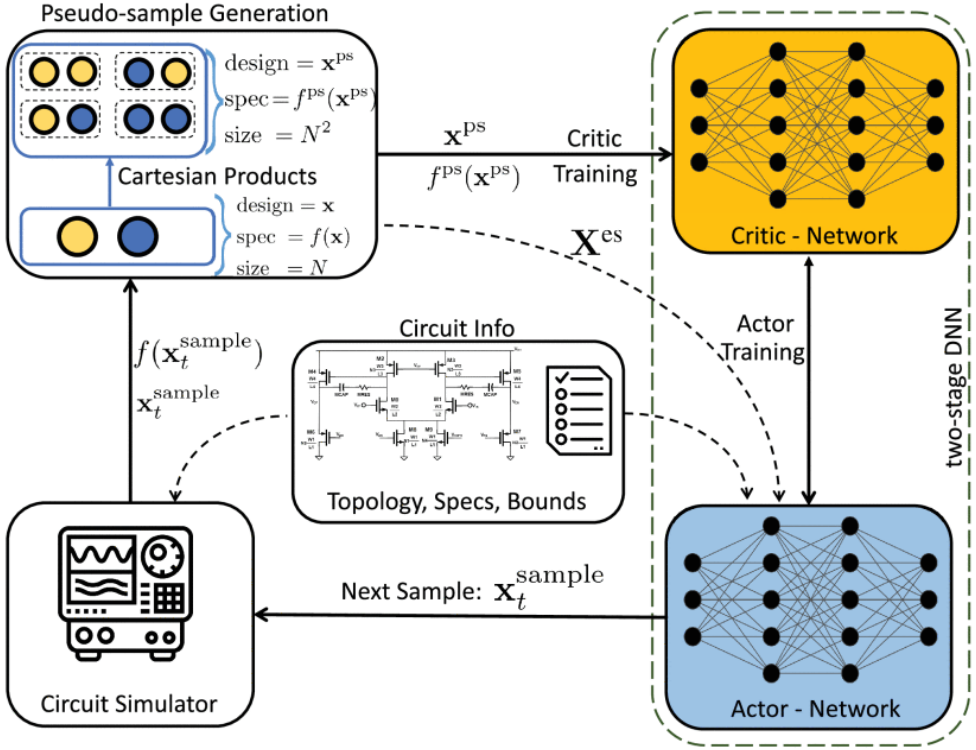
IEEE SPECTRUM AUGUST 1988

Knowledge-based systems are relieving the labor-intensive bottlenecks usually associated with such building blocks as op amps and voltage references

In a matter of hours rather than weeks or months, basic analog integrated circuits can now be designed to suit the needs of the systems they are destined for. This sudden advance is due to new knowledge-based computer-aided design (CAD) tools. With the tools' help, system designers can employ common analog blocks, such as op amps and voltage references, without understanding their operation in much detail. Circuit designers also benefit from having the routine parts of a design done for them.


Idac
Library of unsized-circuit schematics
Design specs
User-selected
User-specified
Simplified analysis equations
Direct solution
Tighten specs
Success?
No
Yes
Sized-circuit schematic
A
Opasyn
Library of unsized-circuit schematics
Design specs
User-selected
User-specified
Complex analysis equations
Nonlinear numerical optimizer
Sized-circuit schematic
B
Oasys
Design specs
User-specified
Higher-level module specifications
Library of design blocks
Highest-level design
Medium-level design
Lowest-level design
Modify topology
Automatic topology choice
Modify equations
Complex analysis equations
Modify plan
Design plan execution
Diagnose failure
No
Success?
Yes
Sized-circuit schematic
Refined submodule specifications
C

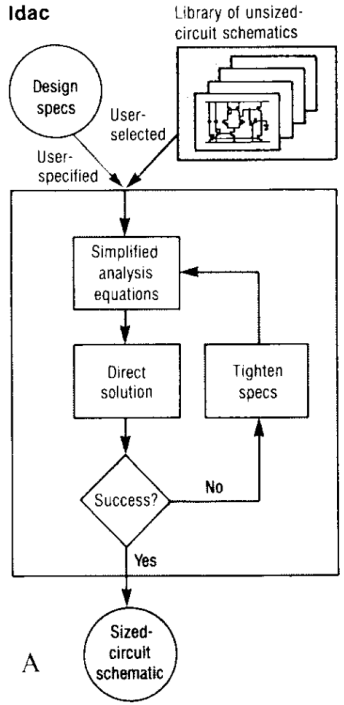
Only Limited Progress 3+ Decades Later…



A. F. Budak et al., "DNN-Opt: An RL Inspired Optimization for Analog Circuit Sizing using Deep Neural Networks," DAC 2021.

What's the Problem?

Major obstacle, often misunderstood and underappreciated!



This is a problem!

"I don't like your opamp"
(e.g., Barcelona Design ✞)
Open-source can help!

This is not the main problem!

A perfectly specified and constrained circuit can be sized very quickly (even by hand!)

It's Complicated…

Highly iterative in both directions, ignored by automation tool designers

Transition is time consuming, difficult to automate

Requirements

"Design a 16x residue amplifier for 14b pipelined SAR ADC"

Topologies

Pick circuit(s) that have a chance to meet specs

Specifications

Can be topology dependent, must consider neighboring blocks & how they evolve

Constraints

Prevent algorithms (or junior designers) to fall into bad local optima

Sizing

Layout

Many automation options exist

Performance/ Quality Assessment

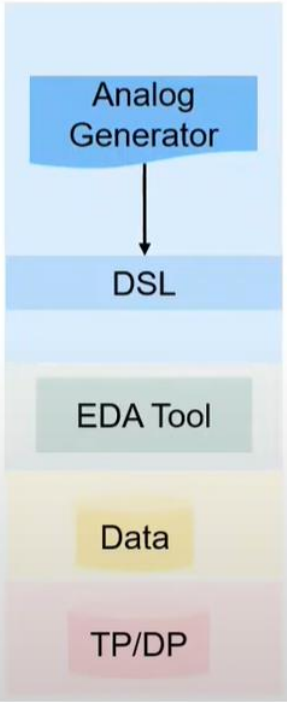
Difficult, especially for layout!

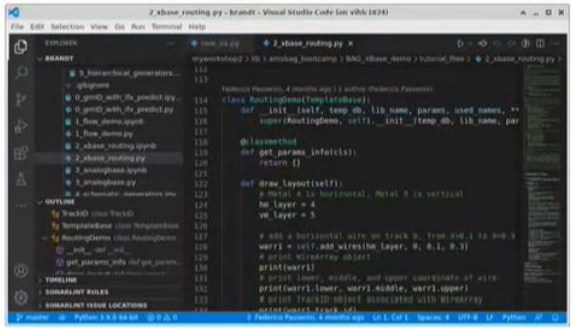
My Perspective

- Full analog design automation (for arbitrary circuits) from requirements to layout is presently not feasible
- We should focus on useful baby steps
  - Build large open-source libraries of proven circuit templates
  - Build a framework that can capture the intent and design steps of an experienced designer → re-use, reproducibility, partial automation
    - BAG, ANAGEN, MOSAIC, …
  - Create fast quality assessment tools for circuits & layouts
    - To enable “big-data” approaches, away from “correct by construction”

ANAGEN

ANAGEN is a **revolution**
for IP design/layout engineer!



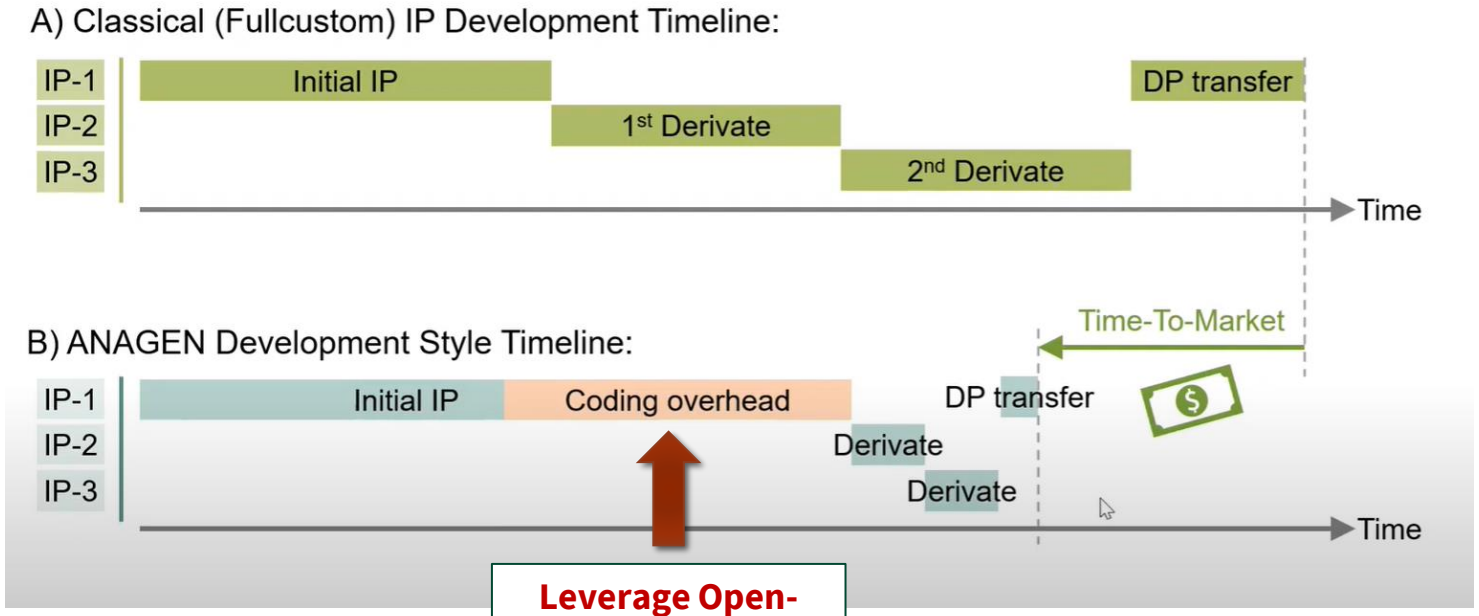


In addition to working with EDA tool, they will need to

- abstract their current manual steps
- translate them into (Python) code
- as general as possible to allow re-use
  - for different technology
  - for different specification

Christoph Sandner, Anagen Motivation, Bootcamp 2022

Addressing Coding Overhead

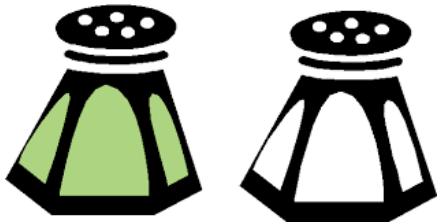


Christoph Sandner, Anagen Motivation, Bootcamp 2022

“I became an analog circuit designer because I don’t like coding”

An amazing opportunity for the next generation of chip designers!

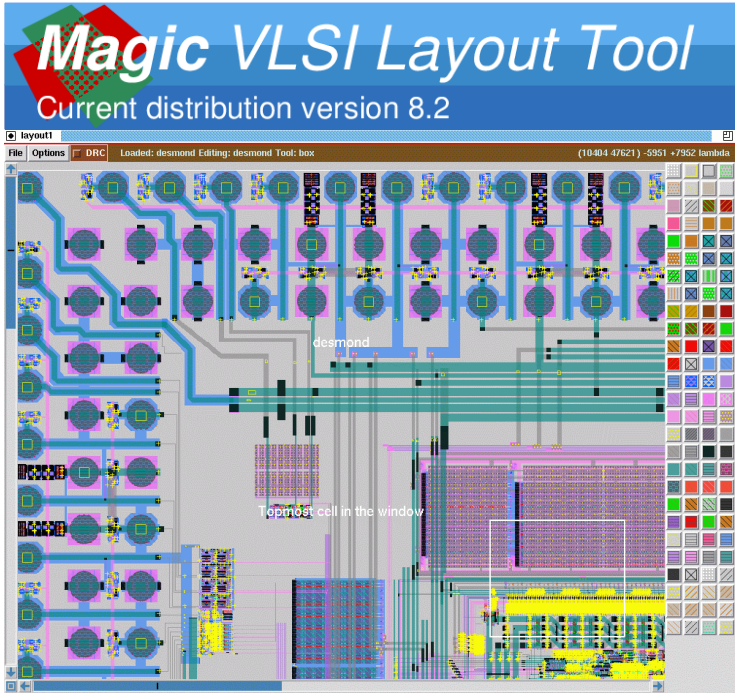
Open-Source is in Our DNA!



SPICE (Simulation Program with Integrated Circuit Emphasis)

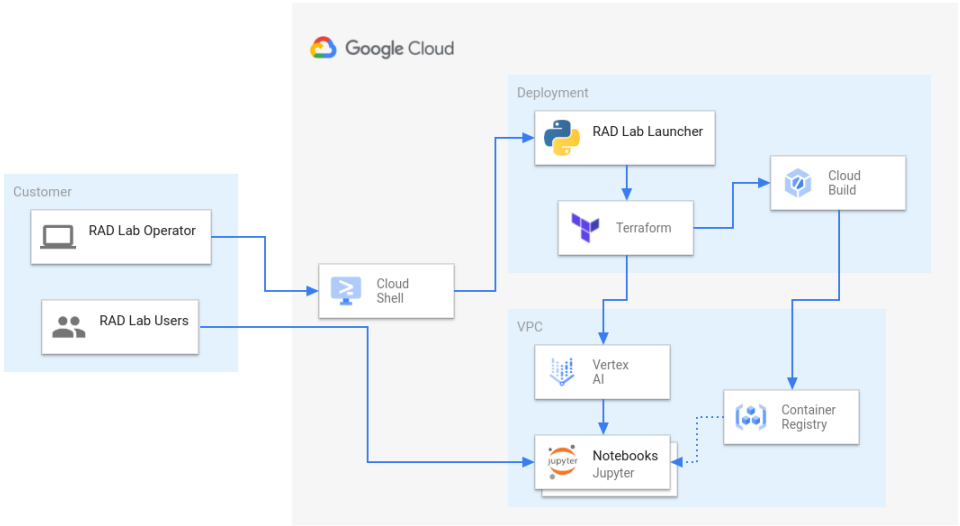
Laurence W. Nagel and D.O. Pederson

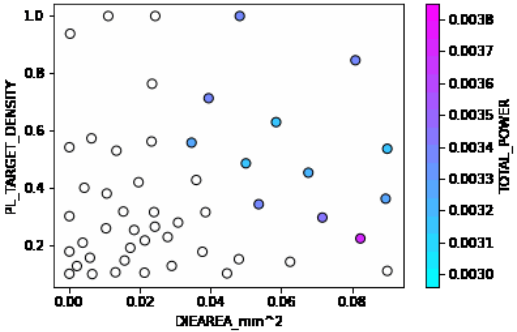
EECS Department
University of California, Berkeley
Technical Report No. UCB/ERL M382
April 1973

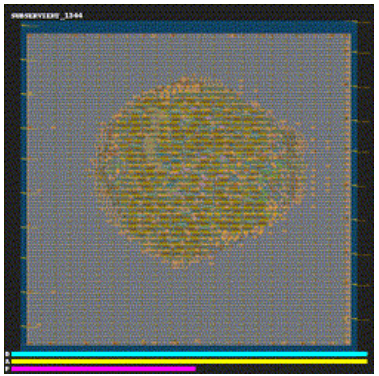


Sources: http://www.omega-enterprises.net, http://opencircuitdesign.com/magic

Open-Source Opens up Amazing New Capabilities!







https://bit.ly/jupyter-silicon

Summary

- There is enormous excitement about collaborative, open-source IC design
  - It will likely change the way we teach & work
  - Fast growing community of >5000 enthusiasts
- The honeymoon period of this development has been fun
  - Community building, free silicon, design contests…
- The next phase comes with an opportunity to revolutionize IC design
  - Creation of platforms for reproducible & re-usable design
  - Difficult to develop in a silo; leverage open-source community!
- Let’s all work together to add a new fun factor to IC design!