



SILVACO

SPICE Modeling of Si, GaN and SiC Power FET Devices 2023 MOS-AK

Bogdan Tudor

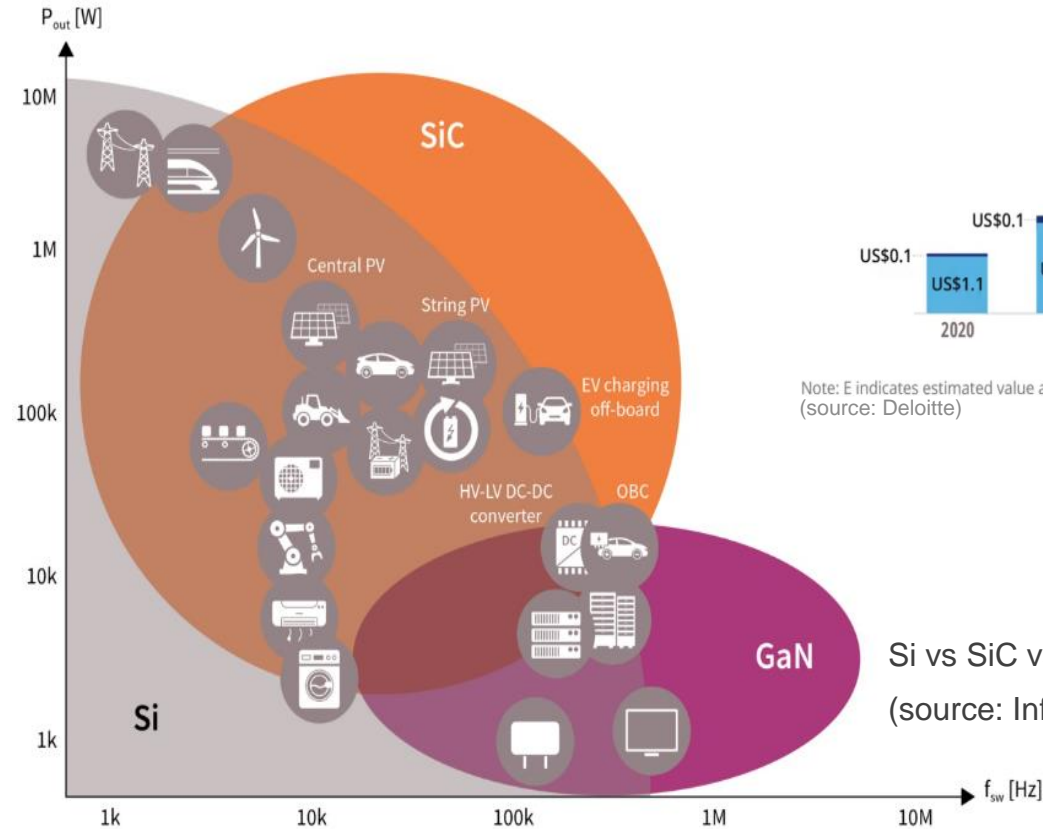
December 2023

Contents

- Introduction
- SPICE Models for GaN and SiC FET
- Modeling Power FET-specific Capacitances
- General Power FET Model Extraction Methodology
- Advantages of TCAD-based SPICE Modeling
- SPICE Modeling Examples of Si, GaN and SiC Devices
- Conclusions

Introduction: Power Device Technologies

- Power applications: Si replaced by Wide Bandgap Semiconductors
- WBG advantages
 - Lower resistance
 - Higher frequency
 - Higher power
 - Higher operating temperature



Annual combined sales of silicon carbide (SiC) and gallium nitride (GaN) power semiconductors (US\$ billions)

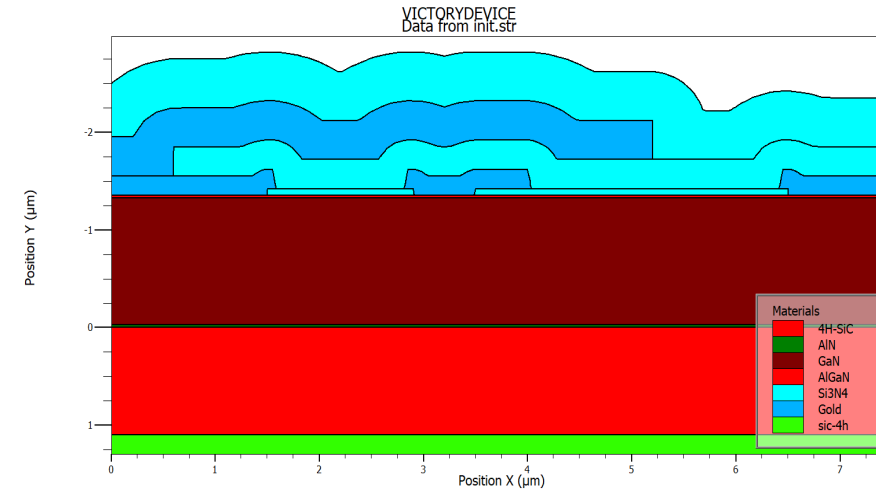
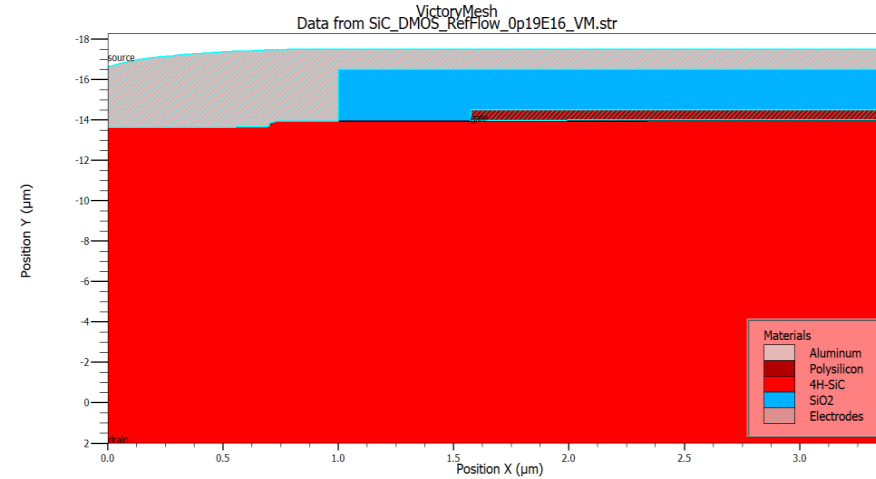


Note: E indicates estimated value and P indicates predicted value.
(source: Deloitte)

SiC and GaN

- SiC
 - Low thermal conductivity
 - High power
 - Main market: automotive/EV

- GaN
 - RF applications
 - Switch-mode power supplies
 - Main market: consumer electronics chargers



SILVACO in Power FET Compact Model Development

CEA-Leti and Silvaco Look to Develop Innovative SPICE Models

Santa Clara, California

Si2 Approves Two IC Design Simulation Standards for Gallium Nitride Devices
 2018 / in Compact Model, Frontpage / by Phillip Isenhart

Si2 Approves Two IC Design Simulation Standards for Fast-Growing Gallium Nitride Market

Compact Model Coalition Models Expected to Reduce Costs, Speed Time-to-Market

For Immediate Release

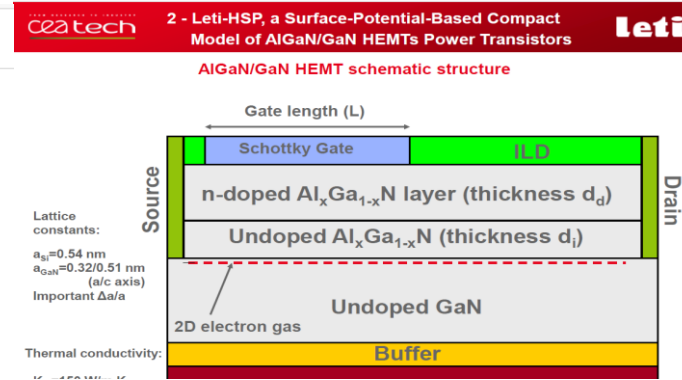
AUSTIN—The Silicon Integration Initiative’s (Si2) Compact Model Coalition market for gallium nitride semiconductors.

The approved standards are the 12th and 13th models currently funded (Simulation Program with Integrated Circuit Emphasis) models for IC design.

John Ellis, president and CEO, said gallium nitride devices are used in major broadband wireless systems, and automotive. “Although it’s currently a slow

To reduce research and development costs and increase simulation accuracy, models. Si2 is a research and development joint venture focused on IC design incorporated into design tools widely used by the semiconductor industry leading universities and national laboratories. The CMC directs and funds:

Dr. Ana Villamor, technology and market analyst at Yole Développement. We project an explosion of this market with 79% CAGR between 2017 and



Left to Right Iliya Pesic, Silvaco Chairman, Emmanuel Sabonnadière, CEA-Leti CEO sign collaboration agreement to develop innovative

Silicon Integration Initiative Targets New Silicon Carbide Standard SPICE Model

April 27, 2021 / in Compact Model, Frontpage / by Terry Berke

The Si2 Compact Model Coalition has voted to fund and standardize a SPICE model for silicon carbide-based metal-on-silicon field-effect transistors. Featuring high efficiency and fast operation with low switching losses, silicon carbide-based metal-on-silicon-field effect transistors are popular in high-growth semiconductor applications such as photovoltaic inverters and converters, industrial motor drives, electric vehicle powertrain and EV charging, and power supply and distribution.



Peter Lee



Colin Shaw

A CMC working group will oversee the model development as part of advancing Si2’s mission to reduce interoperability costs, said Peter Lee, CMC chair. Participating companies include Analog Devices, Cadence Design Systems, Infineon, Qualcomm, Siemens EDA, Silvaco and Synopsys. The decision to launch the working group came after the CMC evaluated the model’s ROI for members and interest by the industry at large. “I’d encourage companies with a stake in SiC devices to join this effort and help guide selection of the model which best represents their intended use,” advised Lee. “They can benefit from both cost reduction that comes from shared model support and a standardized and qualified model that has ongoing bug fixes and requested feature enhancements from many like-minded companies.”

“Next Generation SiC MOSFETS has many features that make them suitable, and even superior to legacy silicon solutions, for several high voltage applications. While the devices can handle high-temperature and voltage, its minimal ON-resistance allows smaller packages and better energy savings than comparable silicon devices,” stated Colin Shaw from Silvaco, the working group chair.

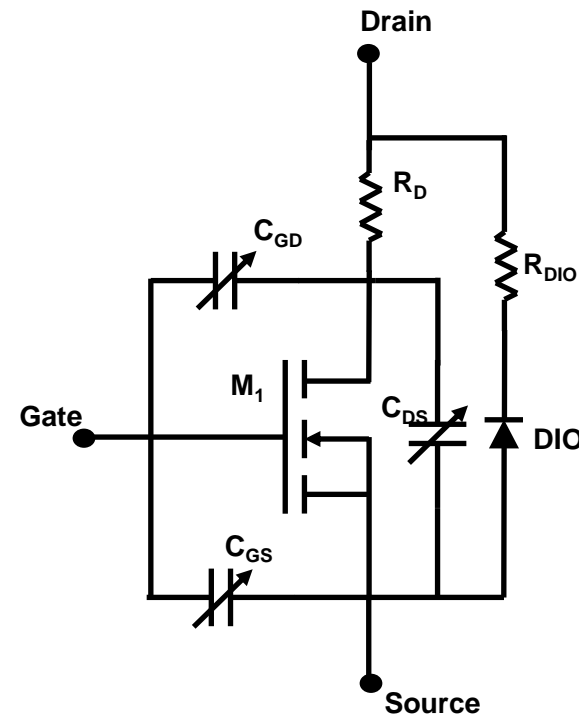
GaN FET: 2 CMC Standard Models

- GaN FET models in SmartSpice:
 - ASM (CMC Standard, SmartSpice Level 90)
 - MVSG (CMC Standard, SmartSpice Level 91)
 - LETI-HSP (SmartSpice Level 278)
- Model extraction initially based on Verilog-A, currently using SmartSpice built-in models
- GaN FET Model Extraction Examples:
 - MVSG: <https://silvaco.com/examples/utmost4/section1/example18/index.html>
 - ASM: <https://silvaco.com/examples/utmost4/section1/example23/index.html>
- GaN FET Model Extraction Webinars:
 - <https://silvaco.com/webinar/tcad-based-model-extraction-flow-for-gan-hemt-devices-part-1-2/>
 - <https://silvaco.com/webinar/tcad-based-model-extraction-flow-for-gan-hemt-devices-part-2-2/>

Template Categories	Quick-Start Templates
MOSFET	BSIM3v3, BSIM4, BSIM-BULK, HiSIM2, HiSIM_HV2, PSP
GaN HEMT	ASM, MVSG
TFT	RPI poly-Si TFT, RPI amorphous Si TFT
BJT	Gummel-Poon, VBIC, Mextram
IGBT	HiSIM_IGBT
Diode	Diode Level 1

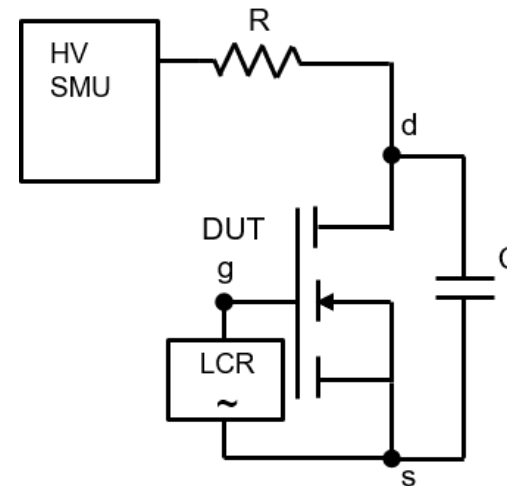
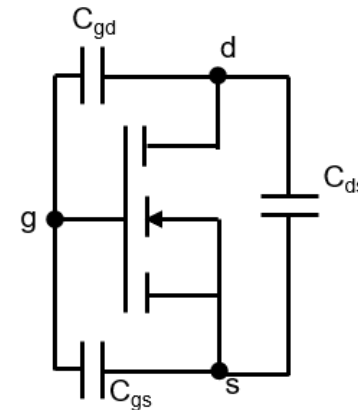
SiC MOSFET SPICE Model Solutions

- CMC SiC compact model standardization currently ongoing
 - Chaired by Silvaco
- Empirical Macromodels
 - Based on behavioral circuit elements (controlled sources, behavioral or PWL capacitors and resistors, etc.)
 - Limited accuracy and predictability
- Use a GaN HEMT model, such as ASM or MVSG
 - Device similarities resulting in a good accuracy and predictability
 - Accuracy can be further improved by using a macromodel
- MOSFET-based macromodel
 - Core FET (e.g., BSIM4)
 - Recovery diode
 - Additional resistors and bias dependent capacitors
 - Reasonable accuracy and predictability



Specific Power MOSFET Capacitances

- 3-terminal MOSFET
 - The b and s nodes are always connected together
- Main bias sweep is V_{ds}
- Typical capacitances to measure:
 - $C_{rss} = C_{gd}$
 - $C_{oss} = C_{gd} + C_{ds}$
 - $C_{iss} = C_{gs} + C_{gd}$
- C_{iss} requires a special test circuit
 - Need to use a corresponding netlist



Single Netlist Supporting All Data

- Use attributes to help distinguish the netlist
 - The Ciss data set includes a special attribute set to 1
 - Conditional netlist based on the attribute value

Netlist

Node Names :

D
G
S

Attribute Names :

W
L
cissvd_flag

Netlist :

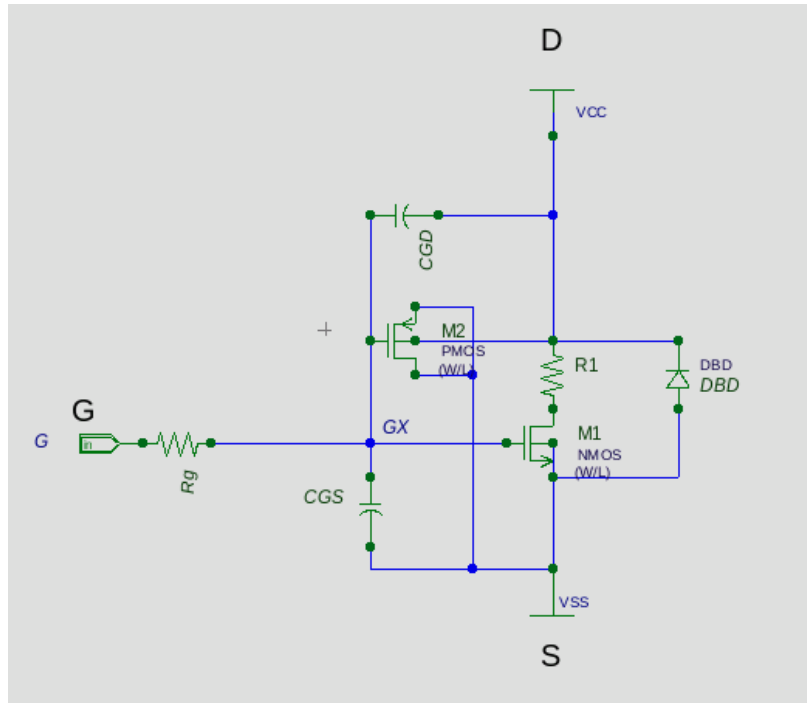
```
IF (cissvd_flag > 0)
R0 D D1 100k
C0 D1 S 10u
X1 D1 G S Power W='W' L='L'

.ELSE
X1 D G S Power W='W' L='L'

.ENDIF
```

Export ... OK Cancel Apply

Power MOSFET Macromodel Example



Model Library : C:/Silvaco/UTMOST4/Examples/Power_SOP_v3/prj_uds/Opt_Power_ok.prj

Model Parameter Simulation

Model Name : NMOS Type : NMOS 8 marked of 13 total Find : Go

Mark	PARAMS	Optimized *	Fit Initial	User Initial	Minimum	Maximum
1	DBD	3	3	3	3	3
2	NMOS	25	25	25		
3	TOX	42.2n	42.2n	42.2n	1n	100n
4	NSUB	3e+17	3e+17			
5	GAMMA	0	0			
6	VTO	1.5	1.5			
7	UO	100	100			
8	ETA	0	0			
9	KP	10u	10u			
10	VMAX	100k	100k			
11	KAPPA	10m	10m			
12	RS	0	0			
13	IS	1p	1p			
14	NFS	1T	1T			
15	TPG	1	1			
16	LD	0	0			
17	CGDO	0	0			

Netlist

Node Names : D, G, S
Attribute Names : W, L, cissvd_flag

```

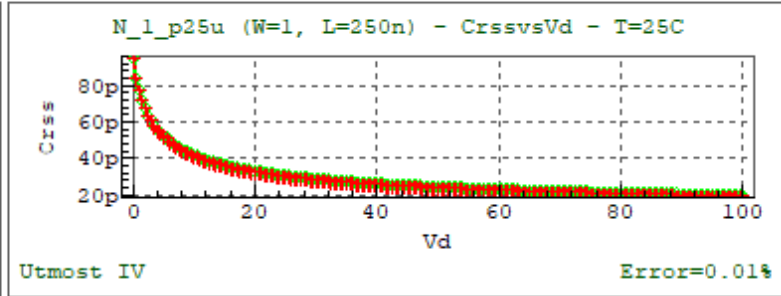
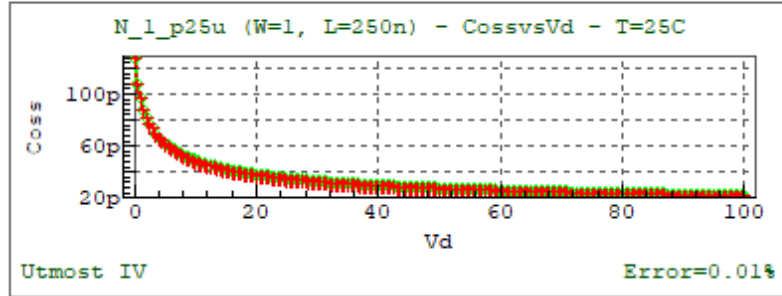
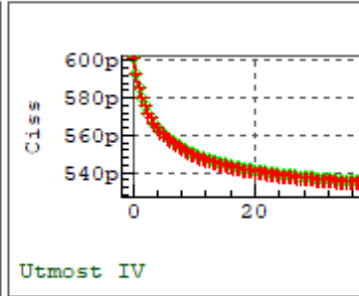
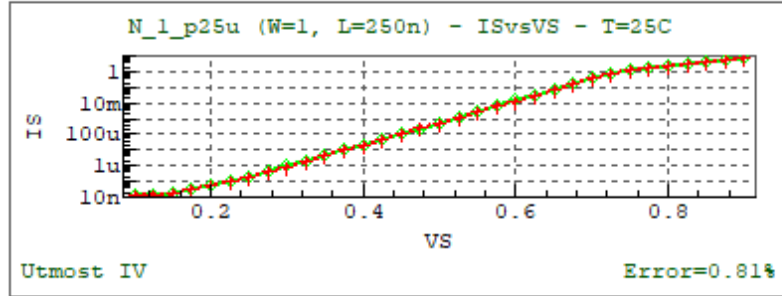
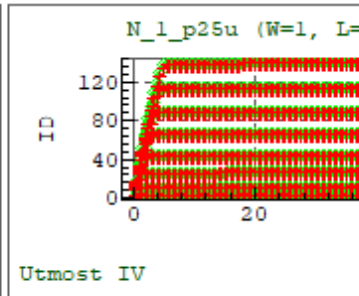
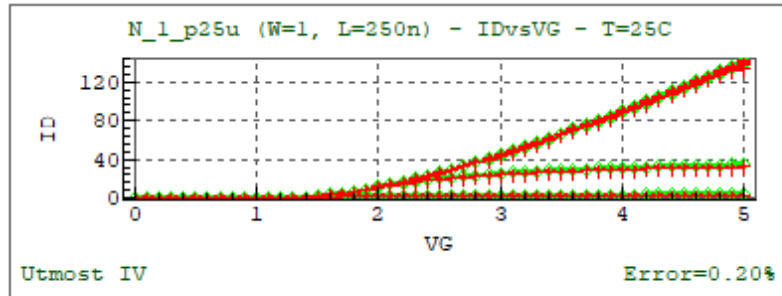
.Netlist :
.IF (cissvd_flag > 0)
R0 D D 100k
C0 D1 S 10u
X1 D1 G S Power W='W' L='L'
.ELSE
X1 D G S Power W='W' L='L'
.ENDIF
.SUBCKT Power D G S W=1 L=1u
M1 D1 GX S S NMOS W='W' L='L'
M2 S GX S D PMOS W='W' L='ratio*L'
R1 D D1 '1' TC=2.534e-03, -3.230e-07
CGS GX S 'cgs'
CGD GX D 'cgd'

```

Export ... OK Cancel Apply

Macromodel I-V and C-V Parameter Extraction

- Global I-V and C-V parameter optimization using Utmost IV



Rubber Band Optimization ✕

Model : DBD Optimized Parameters : Error : 0.13%

Model/Parameter	Value	Minimum	Maximum
PARAMS/cgd	8.34652p	100f	1n
PARAMS/cgs	300.888p	100f	1n
PMOS/NSUB	1.22032e+16	1e+15	1e+17
NMOS/VTO	1.15112	-1	2
NMOS/UO	792.192	10	800
NMOS/ETA	26.3441n	0	1
NMOS/KP	10.0086u	10u	100m
NMOS/VMAX	980.75k	1k	1M
NMOS/KAPPA	2.30729m	1m	1
DBD/CJO	32.8411p	1f	100p
DBD/WJ	587.524m	500m	1

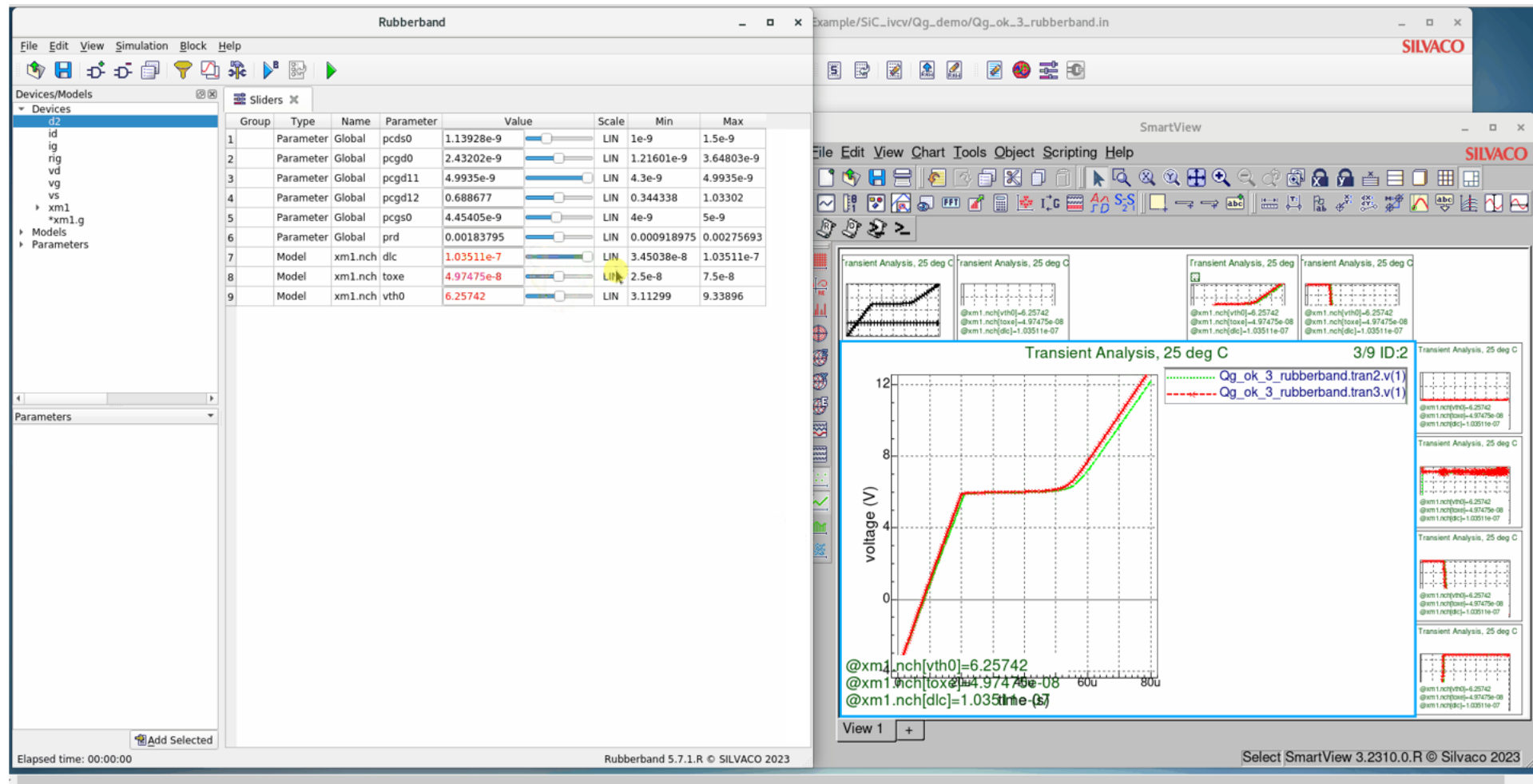
Parameter : LEVEL TNOM IS RS N BV CJO VJ MJ FC

Optimizer : Levenberg-Marquardt

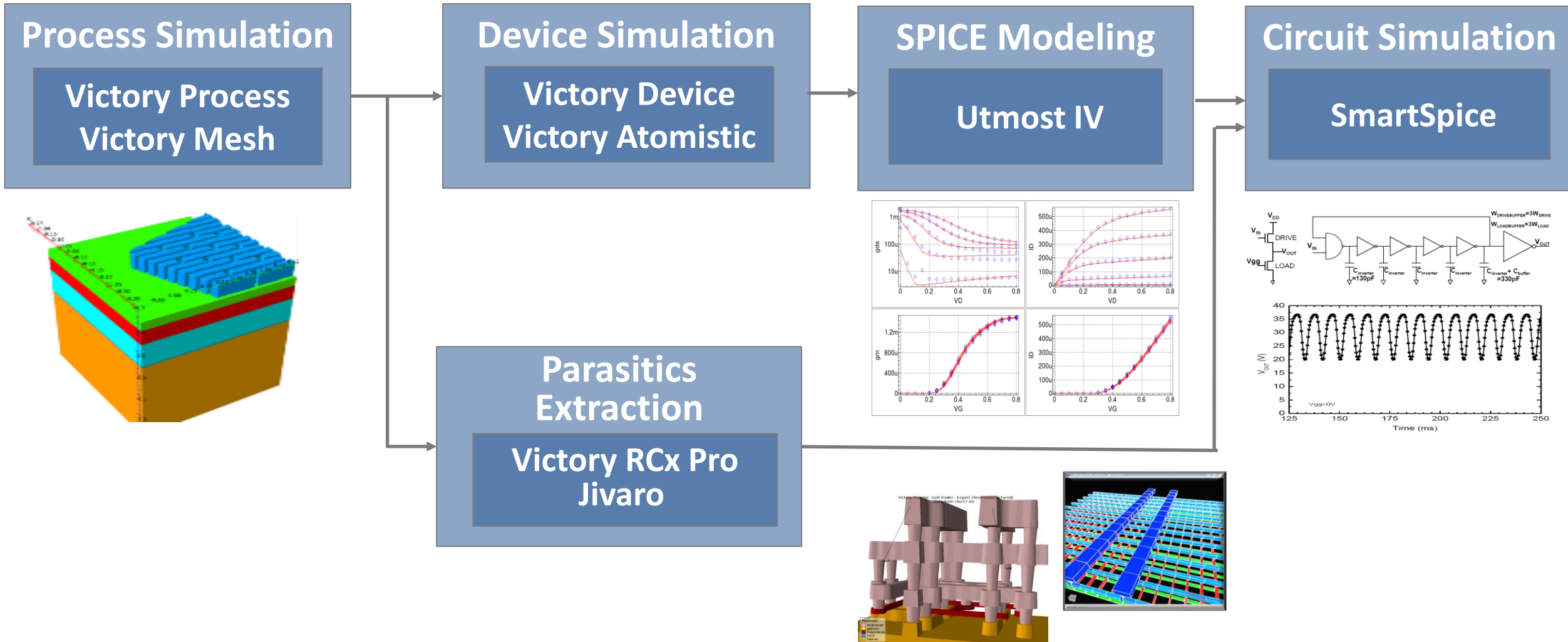
Buttons: Revert, Optimize, OK, Cancel, Apply

Dynamic Characterization

- Using SmartSpice Rubberband to tune Qg

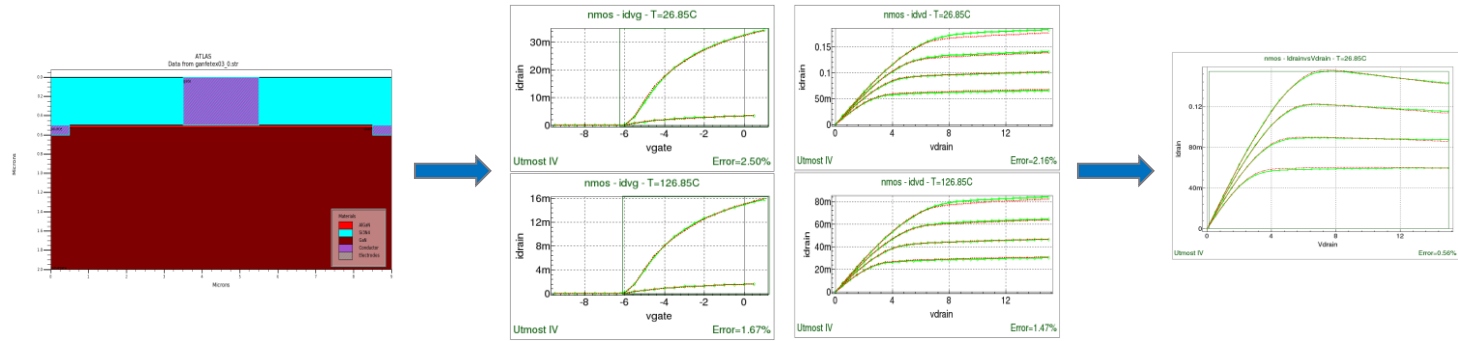


TCAD-to-SPICE DTCO Flow

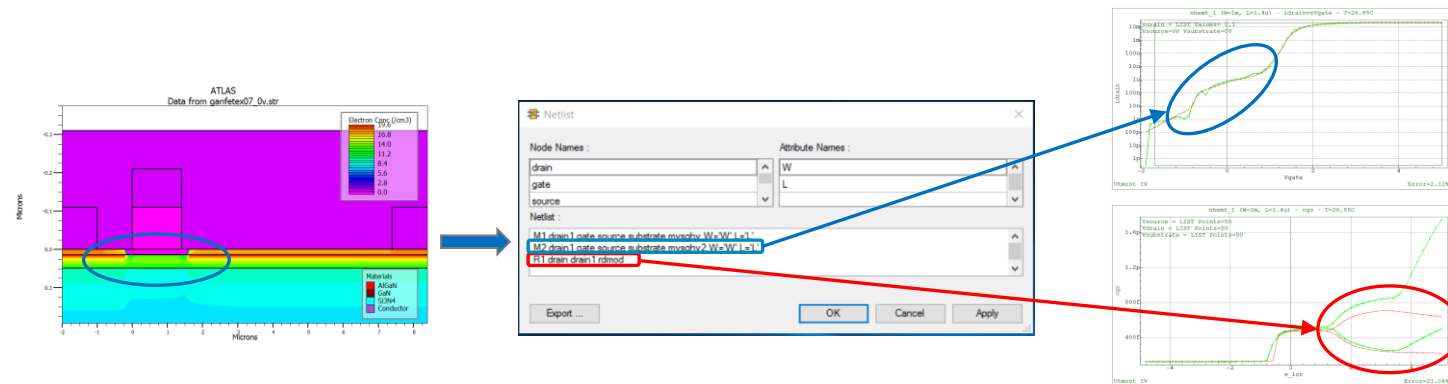


Advantages of TCAD-based SPICE Modeling

- TCAD simulations allows separation of physical effects (e.g., self-heating)

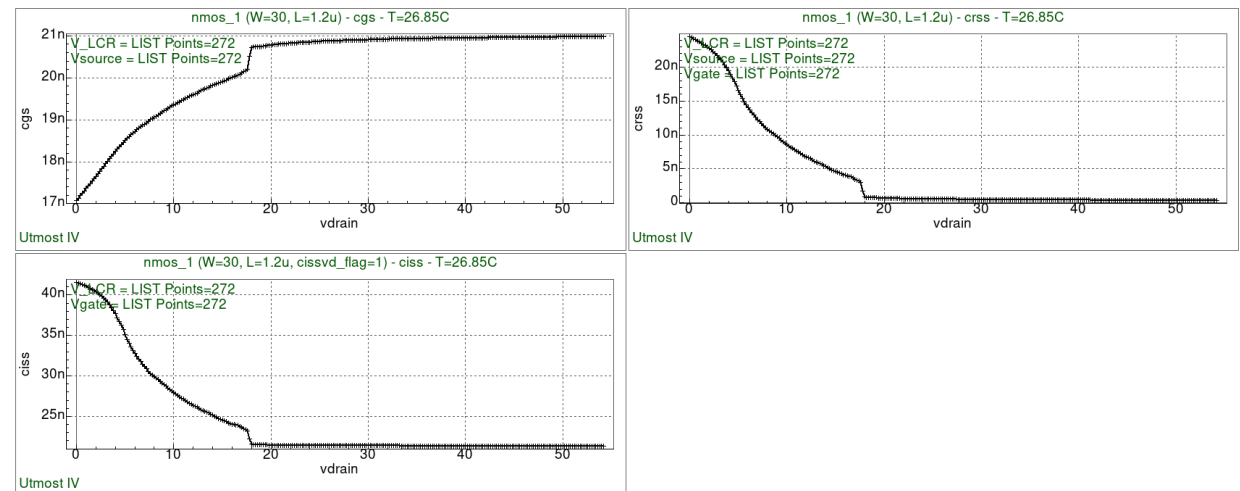
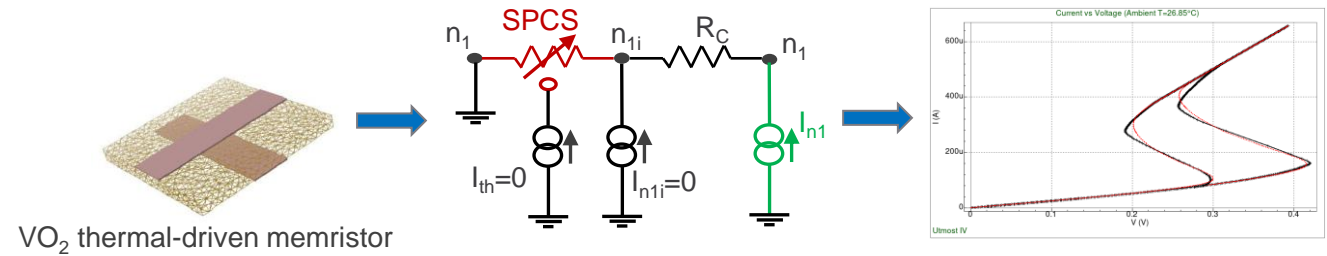
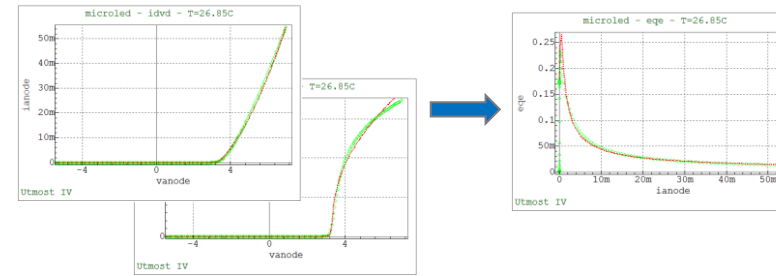


- Model development: identifying specific device effects (or parasitics) and addressing them as SPICE elements



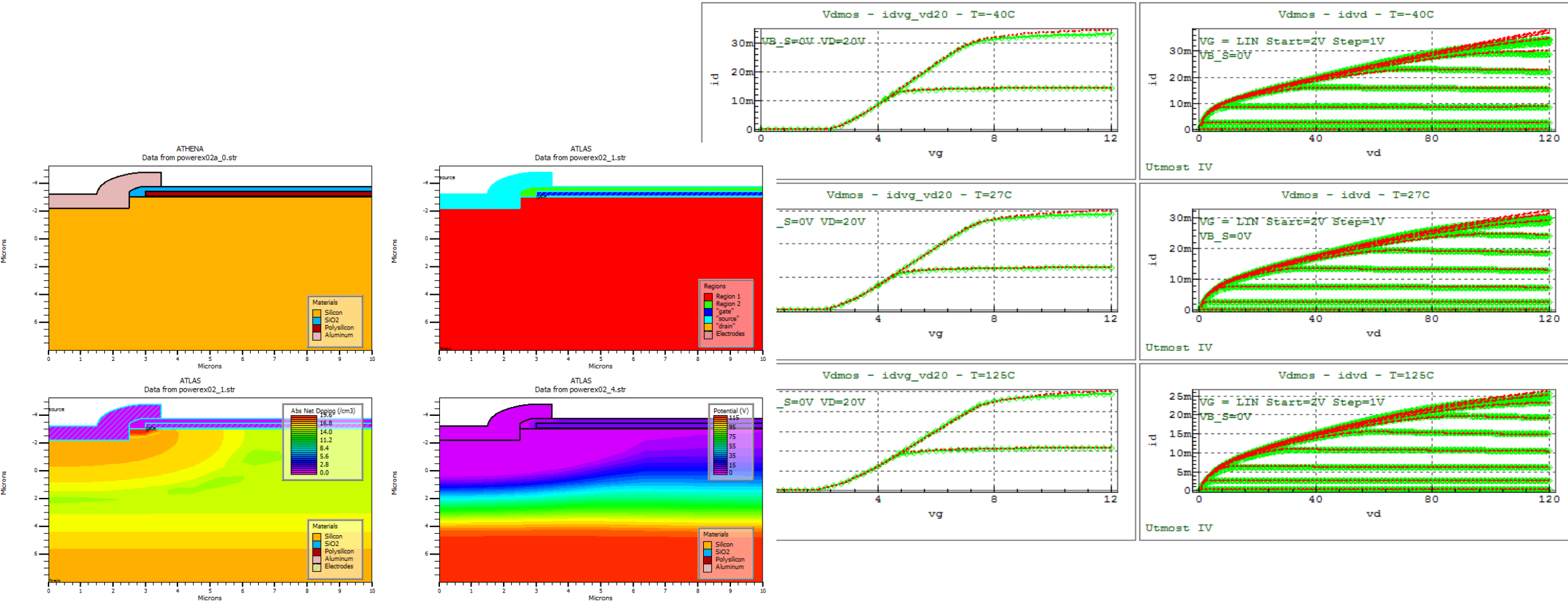
Advantages of TCAD-based SPICE Modeling (2)

- Simulate and calculate critical circuit design-related parameters, that are not easily measurable in real life, e.g.:
 - Probing optical outputs and calculating the Quantum Efficiency of MicroLEDs
 - Probing internal voltage nodes and thermal nodes
- Combining output components to calculate power device-specific quantities
 - Calculate Ciss(Vds) from Cgs(Vds) and Cgd(Vds)



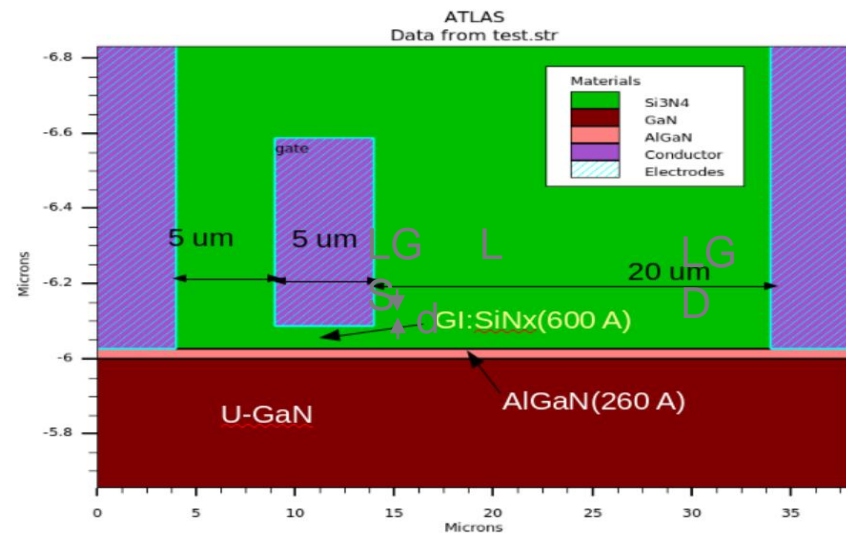
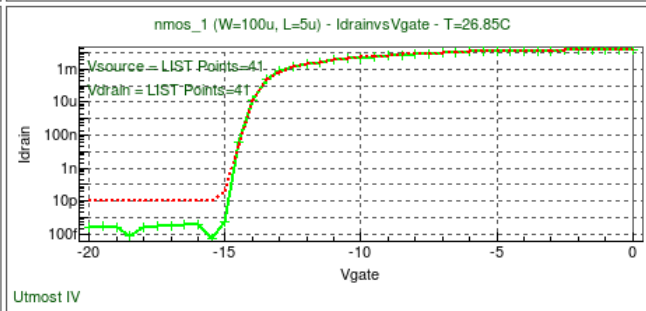
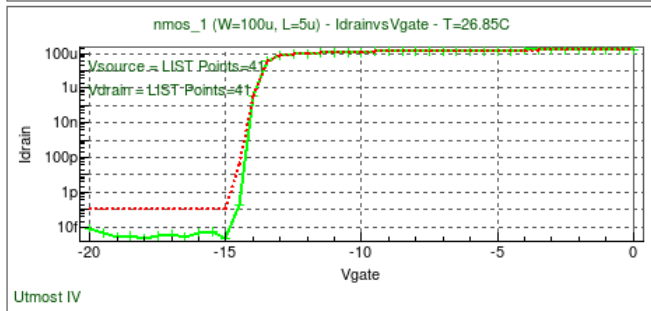
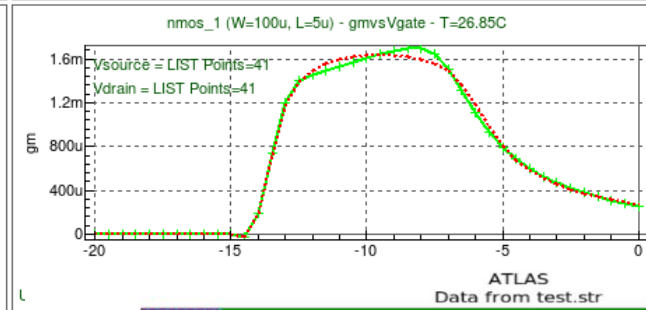
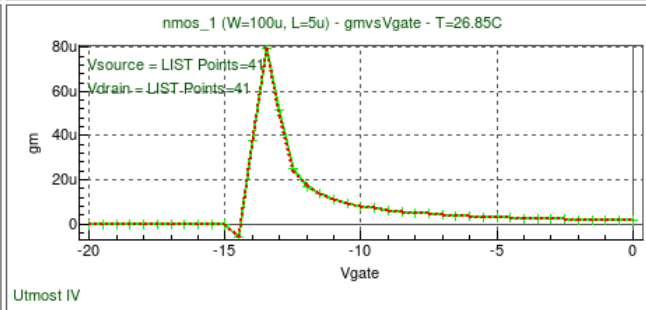
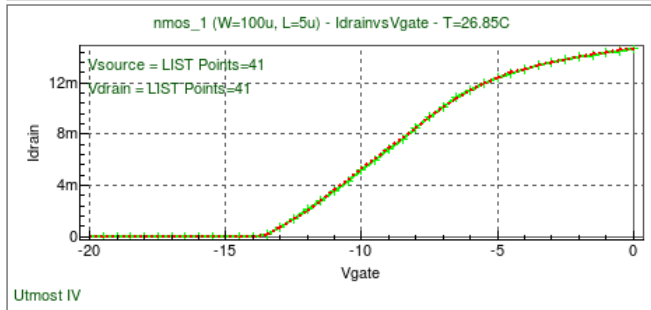
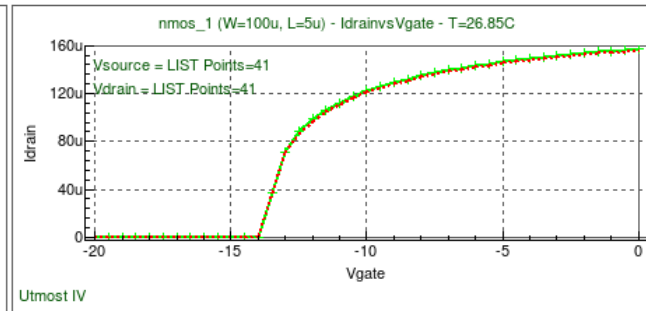
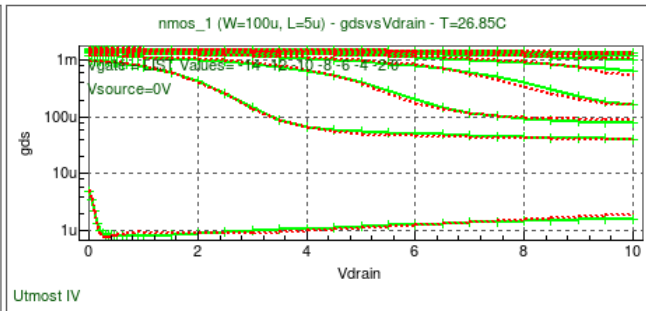
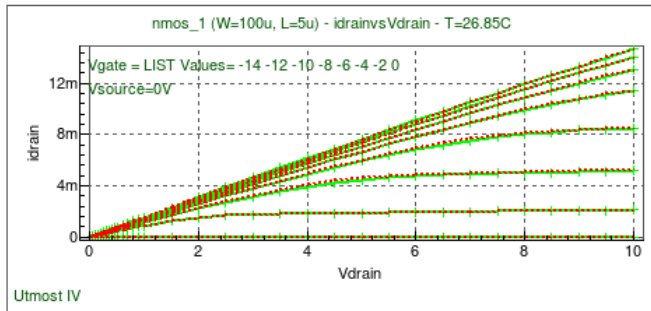
TCAD Si VDMOS Example

- HiSIM_HV2 SPICE Model
- <https://silvaco.com/examples/utmost4/section1/example14/index.html>



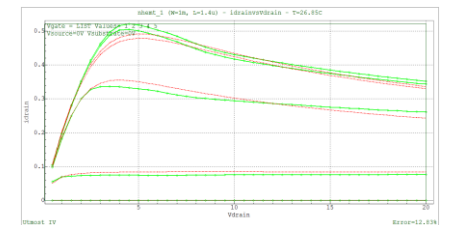
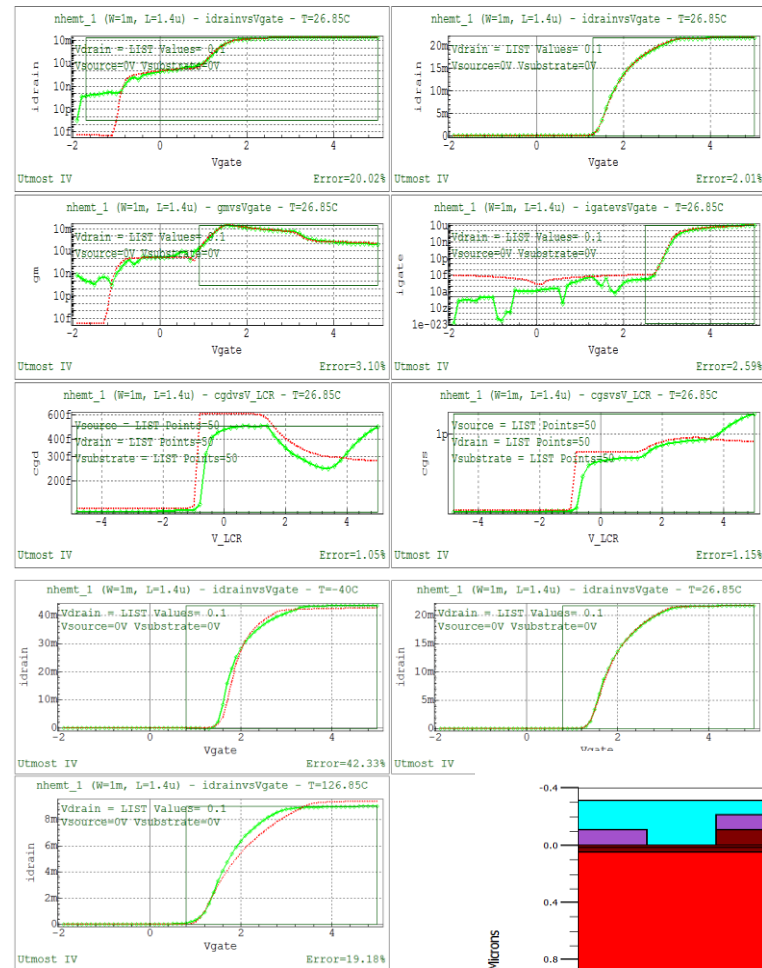
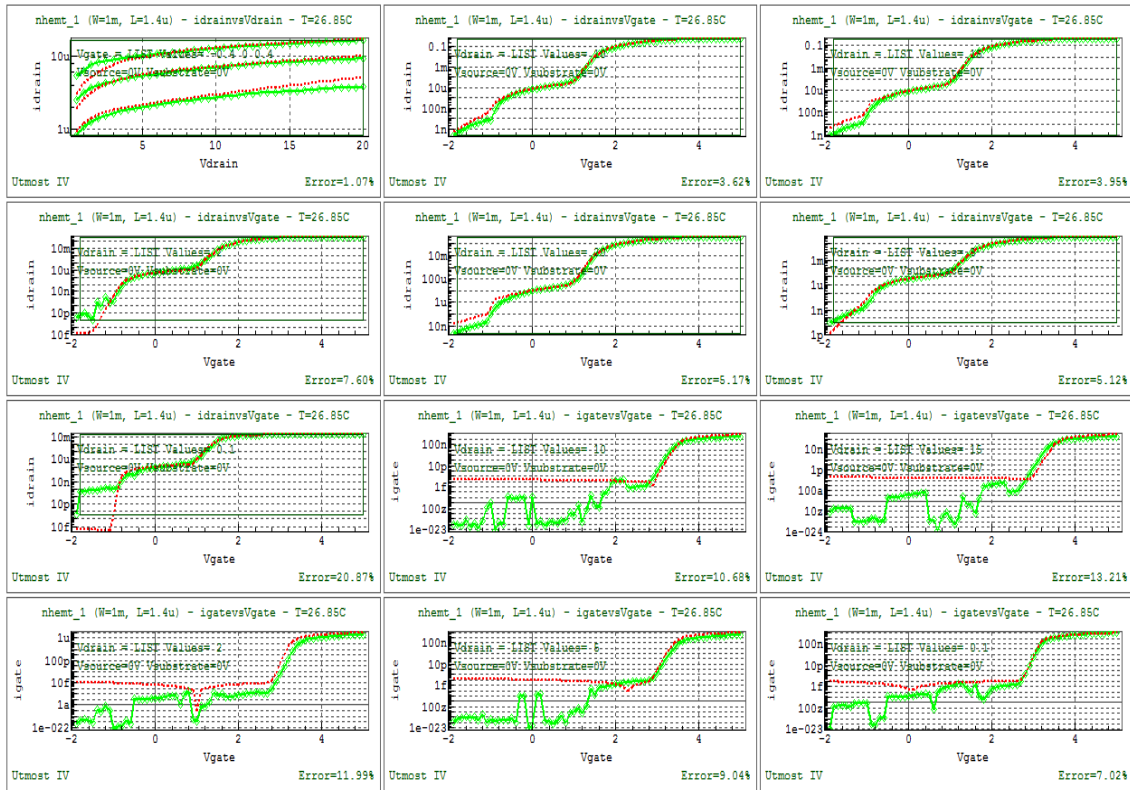
TCAD Generic GaN HEMT Device Structure

- SPICE ASM Compact Model

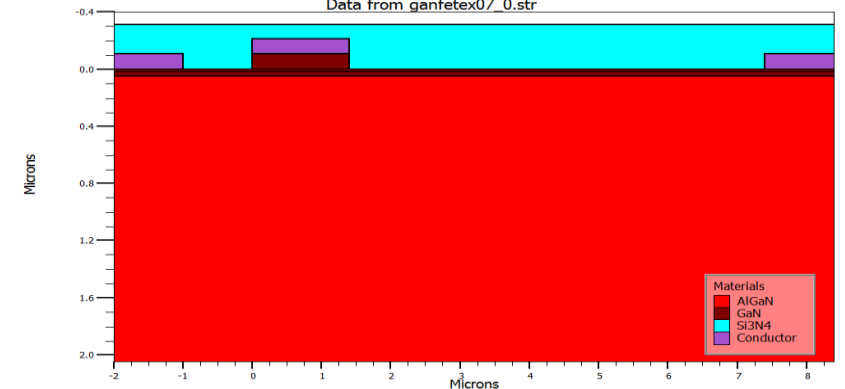


GaN HEMT Device Structure with P-type Gate

- TCAD structure calibrated based on published data
- P-type doped GaN gate resulting in $V_{th} > 0$ ("normally-off" device)

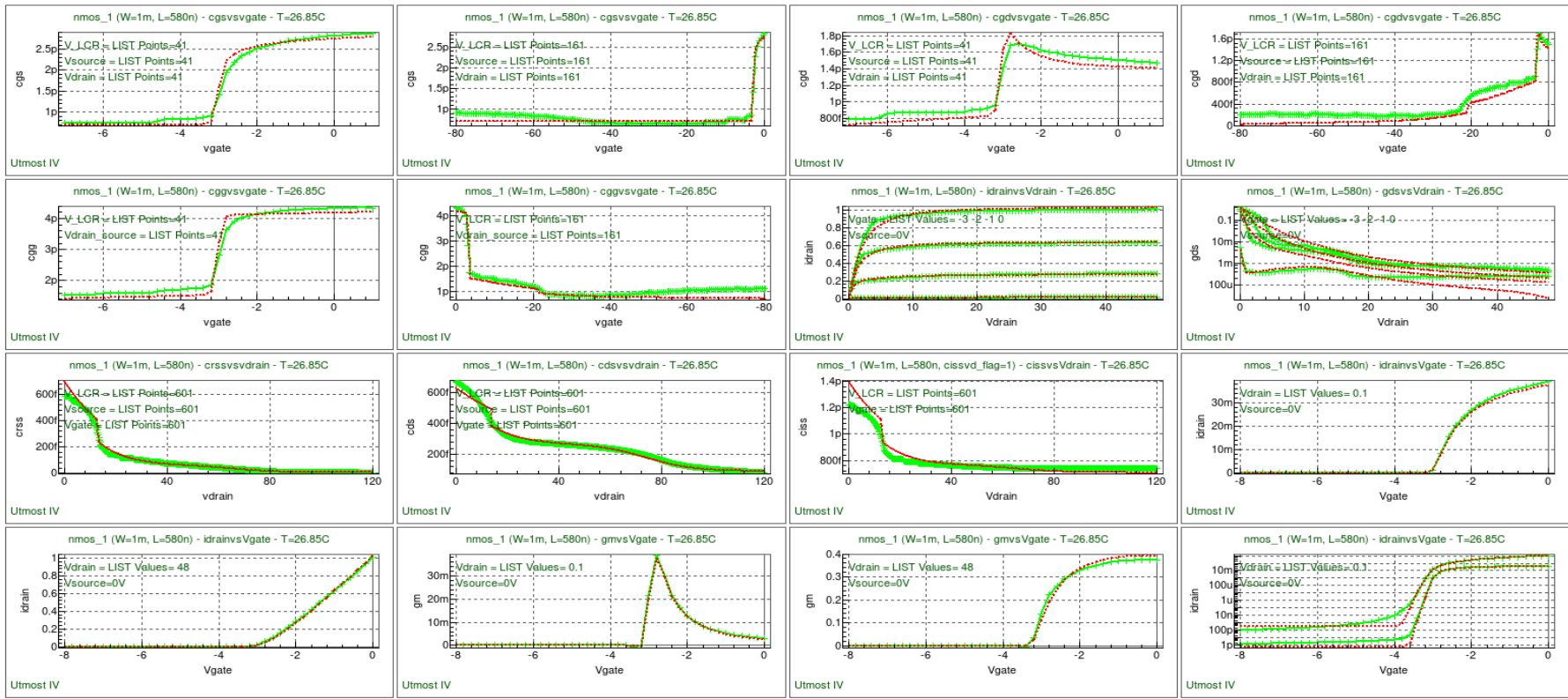
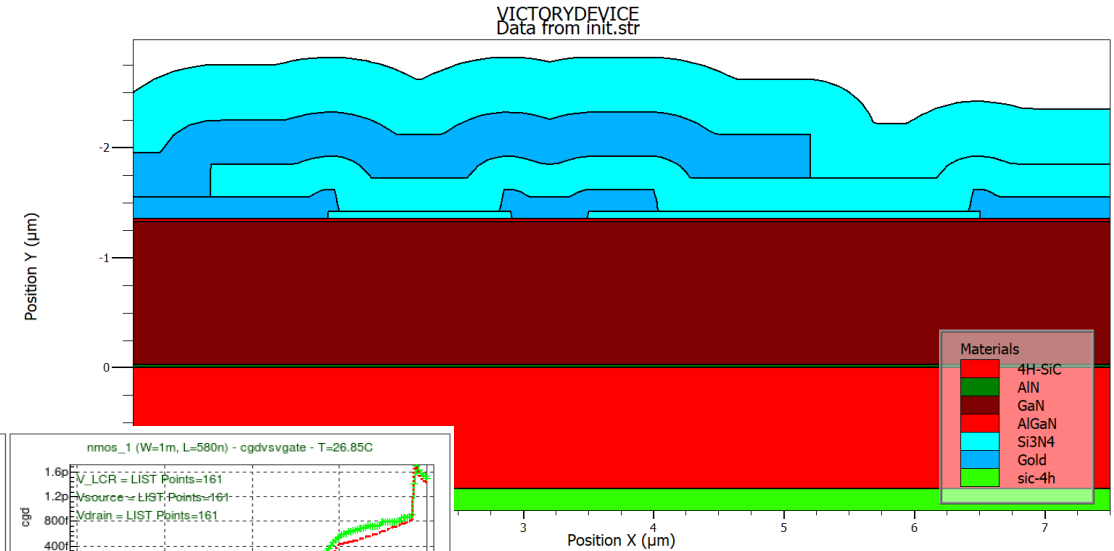


ATLAS
Data from ganfetex07_0.str



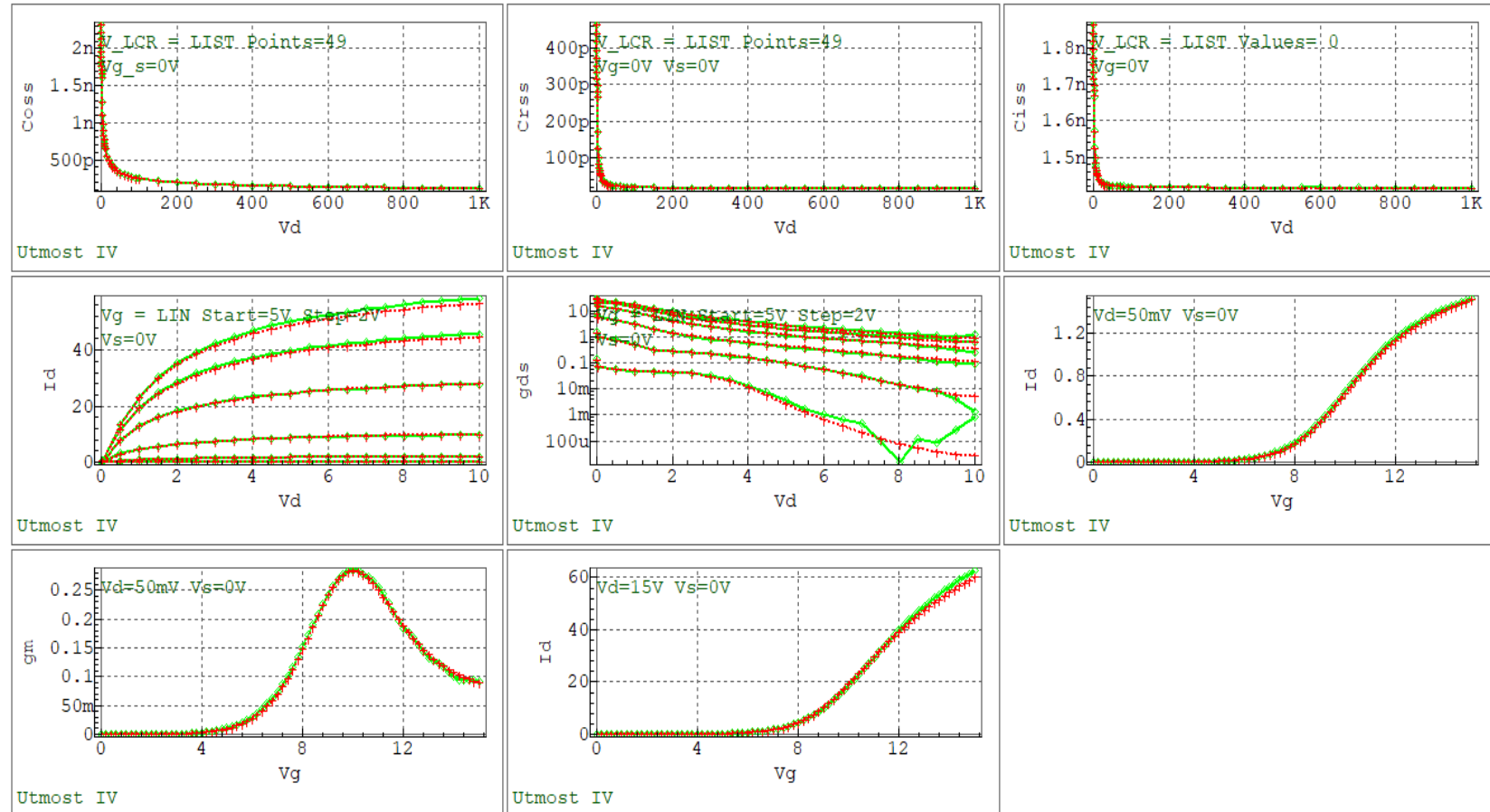
GaN HEMT Device With Field Plates

- TCAD device structure calibrated based on published data
- Gate and source field plates
- SPICE MVSG Compact Model



SiC Macromodel Example

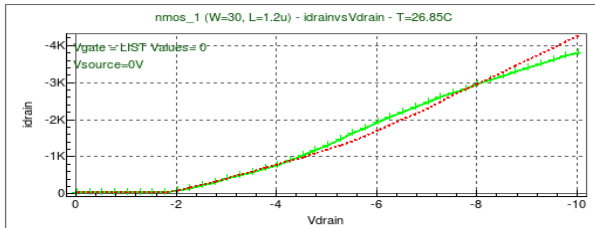
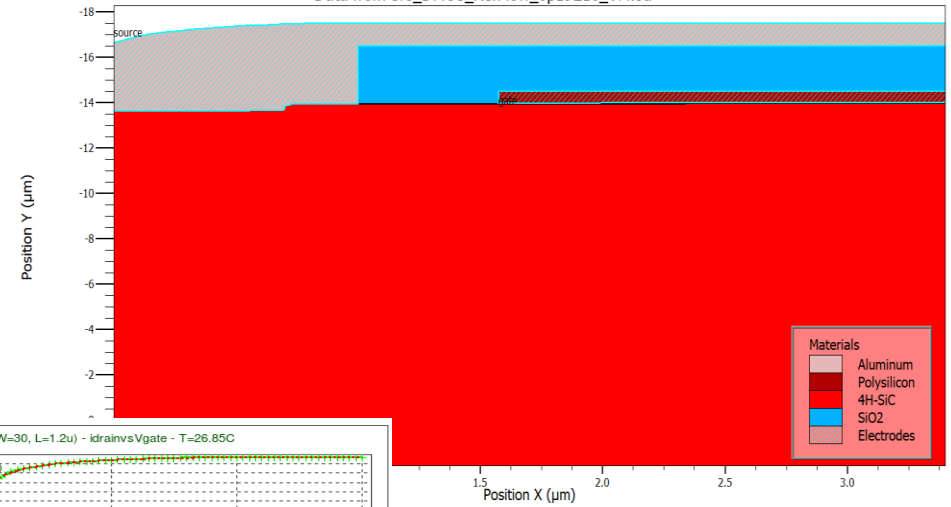
- Based on generic data:
 - C-V: $C_{iss}(V_{ds})$, $C_{rss}(V_{dg})$, $C_{oss}(V_{ds})$
 - I-V: $I_d(V_{gs})$, $I_d(V_{ds})$



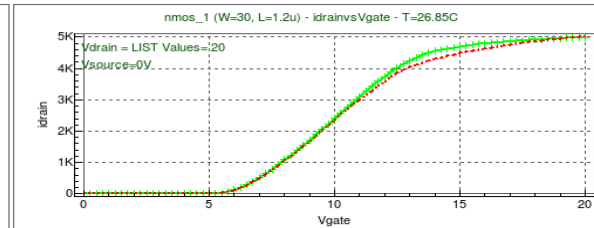
SiC TCAD Device

- TCAD device created using Victory Process, Victory Mesh and Victory Device
- SPICE BSIM4-based Macromodel

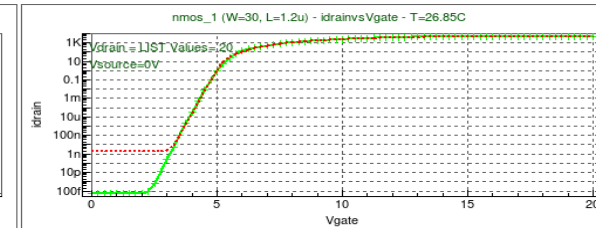
VictoryMesh
Data from SIC_DMOS_RefFlow_0p19E16_VM.str



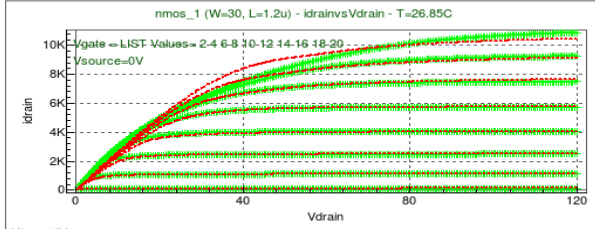
Utmost IV



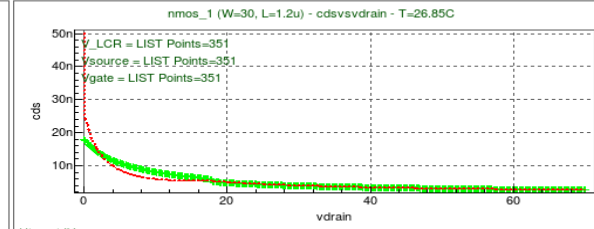
Utmost IV



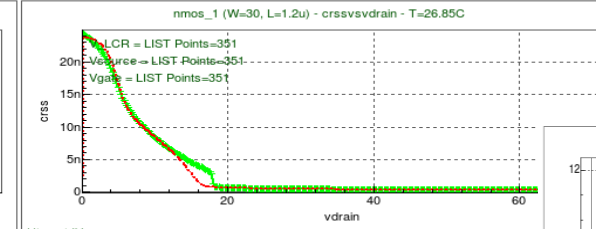
Utmost IV



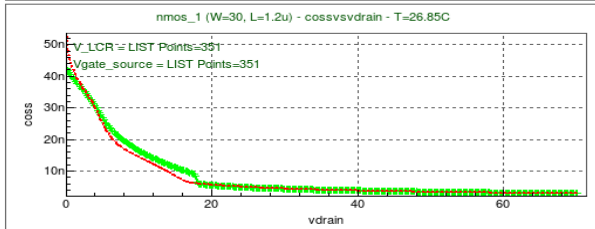
Utmost IV



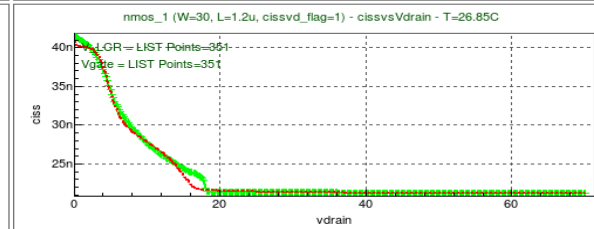
Utmost IV



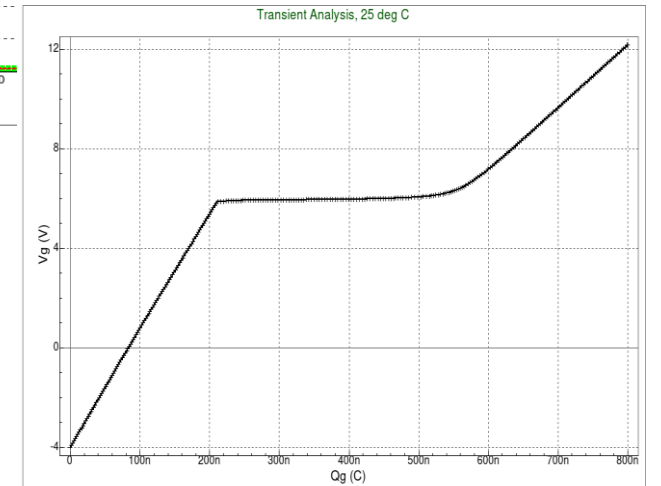
Utmost IV



Utmost IV



Utmost IV



Conclusions

- Review of power device technologies
- Exploration of power FET SPICE models
- Power FET specific capacitance support using a single netlist
- Comprehensive modeling methodology of Power FETs, including dynamic characterization
- TCAD-based SPICE modeling carries unique advantages
- SPICE modeling capabilities addressing various power FET technologies: Si, GaN, SiC
- Silvaco provides a full set of software solutions, from TCAD to SPICE, to address the specific requirements of SPICE modeling for power devices



Thank you

SILVACO