The Analog Designer's Toolbox (ADT)
Towards A New Paradigm for Analog IC Design

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Master Micro LLC and Ain Shams University

adt.master-micro.com
ENIAC, U.S. Army, 1946
Size → Large hall (> 150m²)
Power Consumption ≈ 150kW

Smart phone
Size → Your pocket
Power consumption < 1W
The Transistor and The Integrated Circuit (IC)

First transistor
Dimensions ≈ 100µm
Bell Labs, 1947

Trigate Transistor
Fin width ≈ 8nm
Intel, 2015

First IC
One transistor!
(+ R + C)
TI, 1958

Quad-core CPU
> $10^9$ transistors!
Intel, 2017
The Problem

- Since the release of Berkeley SPICE simulator in the 1970s...
  - No major change in the analog design flow!
- Nanometer transistor models are very complex
  - Tedious multi-variable trial-and-error process on simulation tools...

 Specs

 Square law?

 Simulation results 😞
The Problem

- Since the release of Berkeley SPICE simulator in the 1970s...
  - No major change in the analog design flow!
- Nanometer transistor models are very complex
  - Tedious multi-variable trial-and-error process on simulation tools...
- There is no systematic analog design process!

ADT Talk

- Designer’s productivity 😞
- Sub-optimal solutions 😞
- Poor documentation of the design process 😞
- No transfer of knowledge 😞

Growing chip complexity
Time-to-market
Analog automation efforts have been around since the late 1980s.

But the problem is not yet solved!

- None of these tools managed to acquire widespread acceptance
  - Analog designers still use the manual iterations 50-year-old design methodology

Why?

1. Technical Reasons
2. Psychological Reasons
3. Usage Model Reasons
4. Business Model Reasons
### Technical
- Precomputed look-up tables technology
- Custom vectorized solvers
- Very fast execution time
- Simulator-accurate results

### Psychological
- We are not replacing the designers
- Make the designers more productive.
- Make the design process systematic, optimized, and fun!

### Usage Model
- From Designers... To Designers
- User-friendly designer-oriented interface
- Short learning curve
- Demos and quick-start videos

### Business Model
- Academia and industry
- Free license for academia
- Flexible and affordable licensing model
Outline

- Introduction
- What Is ADT?
- Why ADT?
What Is ADT?

ADT is a new analog EDA tool that is disrupting analog IC design.

ADT enables everyone to reap the benefits of the gm>ID design methodology powered by precomputed LUTs.

Transistor level visualization and automation.

Circuit level visualization and automation.
Outline

- Introduction
- What Is ADT?
  - Transistor Level Visualization and Automation
  - Circuit Level Visualization and Automation
- Why ADT?
Transistor Level: Conventional Flow

- **W, L, VGS**
- **SPICE**
- **Complicated Transistor Models**
- **gm, gm/gds, fT, noise, mismatch, etc.**

- 🙁 50-year-old manual process
- 🙁 Time-consuming
- 🙁 Sub-optimal and non-intuitive
Transistor Level: ADT Flow

Precomputed Lookup Tables

- gm, gm/gds, fT, noise, mismatch, etc.

ADT

- W, L, VGS

Fast
Without SPICE-in-the-loop

Accurate
LUT-based: any simulator/model

Intuitive & Optimized
Visualized and designer-oriented

gm, gm/gds, fT, noise, mismatch, etc.
Outline

- Introduction
- The gm/ID Design Methodology
- What Is ADT?
  - Transistor Level Visualization and Automation
    - ADT Sizing Assistant
    - ADT Device Xplore
  - Circuit Level Visualization and Automation
- Why ADT?
ADT Sizing Assistant: Coming Soon!
Introduction

What Is ADT?
- Transistor Level Visualization and Automation
  - ADT Sizing Assistant
  - ADT Device Xplore
- Circuit Level Visualization and Automation

Why ADT?
Design Example: IGS

\[ GBW = f_u = G_m R_{\text{out}} \times \frac{1}{2\pi R_{\text{out}} C_{\text{out}}} \approx \frac{g_m}{2\pi C_L} \]

\[ g_m = 2\pi C_L \times f_u = 1.257 \text{ mS} \]

- Let

\[ \frac{g_m}{I_D} = 5 \ (\text{SI}) \rightarrow 25 \ (\text{WI}) \]

- Then

\[ I_D \approx 50 \mu A \ (\text{WI}) \rightarrow 250 \mu A \ (\text{SI}) \]

<table>
<thead>
<tr>
<th>Spec</th>
<th>Constraint</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>50</td>
</tr>
<tr>
<td>GBW</td>
<td>200 MHz</td>
</tr>
<tr>
<td>CL</td>
<td>1 pF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DOF</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IB</td>
<td>?</td>
</tr>
<tr>
<td>( g_m / I_D )</td>
<td>?</td>
</tr>
<tr>
<td>L</td>
<td>?</td>
</tr>
</tbody>
</table>
Sweeping gm/ID
**Final Design**

<table>
<thead>
<tr>
<th>DOF</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IB</td>
<td>80 uA</td>
</tr>
<tr>
<td>gm/ID</td>
<td>15.97</td>
</tr>
<tr>
<td>L</td>
<td>0.22 um</td>
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</table>

<table>
<thead>
<tr>
<th>Spec</th>
<th>ADT</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>51.5</td>
<td>51.53</td>
</tr>
<tr>
<td>GBW</td>
<td>200 MHz</td>
<td>199.8 MHz</td>
</tr>
</tbody>
</table>

**DOF Table:**

- **GM/ID:** 15.97
- **GM/GDS:** 51.51
- **L:** 220n

**Graphs:**

- GM/ID vs. GM/GDS
- GBW vs. GM/ID

**Equations:**

\[ \frac{I_B}{v_{in}} \rightarrow v_{out} \]

\[ C_L \]

\[ v_{in} \]

\[ v_{out} \]
Outline

- Introduction
- **What Is ADT?**
  - Transistor Level Visualization and Automation
  - **Circuit Level Visualization and Automation**
- Why ADT?
Circuit Level: Conventional Flow

Complicated Transistor Models

SPICE

Gain  41 dB
Bandwidth  240 kHz
Power  1 mW

😊 50-year-old manual process
😊 Time-consuming
😊 Sub-optimal and non-intuitive
Circuit Level: ADT Flow

Precomputed Lookup Tables

Designer-Oriented Visualization and Optimization

Fast
Without SPICE-in-the-loop

Accurate
LUT-based: any simulator/model

Intuitive & Optimized
Visualized and designer-oriented
Outline

- Introduction
- What Is ADT?
  - Transistor Level Visualization and Automation
  - Circuit Level Visualization and Automation
    - CS Amplifier Using Design Xplore
    - Two-Stage Amplifier Using Design Cockpit
    - Folded Cascode With Capacitive Feedback Optimization
    - BGR Corners and Mismatch Analysis
- Why ADT?
Design Example: Common Source Amplifier

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>50</td>
</tr>
<tr>
<td>GBW</td>
<td>200 MHz</td>
</tr>
<tr>
<td>IB</td>
<td>&lt; 100 uA</td>
</tr>
<tr>
<td>ΣW*L</td>
<td>&lt; 200 um²</td>
</tr>
</tbody>
</table>

![Circuit Diagram]
Design Example: Common Source Amplifier

<table>
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<tr>
<td>DC Gain</td>
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<tr>
<td>GBW</td>
<td>200 MHz</td>
</tr>
<tr>
<td>IB</td>
<td>&lt; 100 uA</td>
</tr>
<tr>
<td>ΣW*L</td>
<td>&lt; 200 um²</td>
</tr>
</tbody>
</table>

\[
\text{vin} - M_2 - V_B - M_1 - v_{out}
\]

<table>
<thead>
<tr>
<th></th>
<th>M1</th>
<th>M2</th>
</tr>
</thead>
<tbody>
<tr>
<td>gm/ID</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>L</td>
<td>↓</td>
<td>↑</td>
</tr>
</tbody>
</table>
Design Tuning: Pick L
Design Tuning: Pick gm/ID
Verification
Outline

- Introduction
- What Is ADT?
  - Transistor Level Visualization and Automation
  - Circuit Level Visualization and Automation
    - CS Amplifier Using Design Xplore
    - Two-Stage Amplifier Using Design Cockpit
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      - BGR Corners and Mismatch Analysis
- Why ADT?
## Design Example: Two-Stage Amplifier

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
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<tbody>
<tr>
<td>DC Gain</td>
<td>60 dB</td>
</tr>
<tr>
<td>GBW</td>
<td>100 MHz</td>
</tr>
<tr>
<td>IB</td>
<td>Min</td>
</tr>
<tr>
<td>PM</td>
<td>What-if?</td>
</tr>
</tbody>
</table>

![Amplifier Circuit Diagram]
What-if?
Outline

- Introduction
- What Is ADT?
  - Transistor Level Visualization and Automation
  - Circuit Level Visualization and Automation
    - CS Amplifier Using Design Xplore
    - Two-Stage Amplifier Using Design Cockpit
    - Folded Cascode With Capacitive Feedback Optimization
    - BGR Corners and Mismatch Analysis
- Why ADT?
Design Example: Capacitive Feedback Amplifier

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>DC LG</td>
<td>&gt; 500</td>
</tr>
<tr>
<td>BW</td>
<td>100 MHz</td>
</tr>
<tr>
<td>PM</td>
<td>70-80 deg</td>
</tr>
<tr>
<td>IB</td>
<td>Min</td>
</tr>
<tr>
<td>RMS noise</td>
<td>Min</td>
</tr>
<tr>
<td>CL DC Gain</td>
<td>2</td>
</tr>
<tr>
<td>CF</td>
<td>500 fF</td>
</tr>
<tr>
<td>CL</td>
<td>500 fF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Variable</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
</tr>
</thead>
<tbody>
<tr>
<td>gm/ID</td>
<td>↑</td>
<td>↓</td>
<td>?</td>
<td>?</td>
<td>↓</td>
</tr>
<tr>
<td>L</td>
<td>↓</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
</tr>
</tbody>
</table>
Optimization

Optimization Settings

- DDB: A010007_1MEG.db
- Properties: Best DDB Point
- Corner: Nominal
- Max No. of Iterations: 10
- Constraints Strictness: Moderate

DOFs

<table>
<thead>
<tr>
<th>Name</th>
<th>Min</th>
<th>Max</th>
<th>Active</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>180n</td>
<td>3u</td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td>60n</td>
<td>3u</td>
<td></td>
</tr>
<tr>
<td>M3</td>
<td>50n</td>
<td>3u</td>
<td></td>
</tr>
<tr>
<td>M4</td>
<td>50n</td>
<td>3u</td>
<td></td>
</tr>
<tr>
<td>M5</td>
<td>50n</td>
<td>3u</td>
<td></td>
</tr>
<tr>
<td>M6</td>
<td>50n</td>
<td>3u</td>
<td></td>
</tr>
</tbody>
</table>

Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Min</th>
<th>Max</th>
<th>Weight</th>
<th>Active</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>100MEG</td>
<td>237.1MEG</td>
<td>1</td>
<td>✔️</td>
</tr>
<tr>
<td>UGF</td>
<td>0.825MEG</td>
<td>344.6MEG</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>PM</td>
<td>79</td>
<td>89</td>
<td>1</td>
<td>✔️</td>
</tr>
<tr>
<td>Static Gain</td>
<td>553.1u</td>
<td>16.37m</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>DC LG</td>
<td>500</td>
<td>1.807k</td>
<td>1</td>
<td>✔️</td>
</tr>
</tbody>
</table>

Objectives

<table>
<thead>
<tr>
<th>Name</th>
<th>Operation</th>
<th>Weight</th>
<th>Active</th>
</tr>
</thead>
<tbody>
<tr>
<td>IB_Nominal</td>
<td>Minimize</td>
<td>1</td>
<td>✔️</td>
</tr>
<tr>
<td>Total Input Integra</td>
<td>Minimize</td>
<td>1</td>
<td>✔️</td>
</tr>
</tbody>
</table>

Optimization Results
Outline

- Introduction
- What Is ADT?
  - Transistor Level Visualization and Automation
  - Circuit Level Visualization and Automation
    - CS Amplifier Using Design Xplore
    - Two-Stage Amplifier Using Design Cockpit
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    - BGR Corners and Mismatch Analysis
- Why ADT?
Design Example: BGR Corners and Mismatch
Outline

- Introduction
- What Is ADT?
  - Transistor Level Visualization and Automation
  - Circuit Level Visualization and Automation
- Why ADT?
Why ADT?

<table>
<thead>
<tr>
<th>Problem</th>
<th>The Solution: ADT</th>
</tr>
</thead>
<tbody>
<tr>
<td>✗ Limited designer’s productivity</td>
<td>✓ Boosts designer’s productivity</td>
</tr>
<tr>
<td>✗ Lost in papers and books to find a good topology</td>
<td>✓ A design library with the most popular circuits invented by analog designers over the years</td>
</tr>
<tr>
<td>✗ Tedious trial-and-error design process.</td>
<td>✓ Intuitive design process.</td>
</tr>
<tr>
<td>✗ Inferior design solutions.</td>
<td>✓ Blazing speed optimization.</td>
</tr>
<tr>
<td>✗ Poor documentation of the design process and no transfer of knowledge and expertise.</td>
<td>✓ Systematic process that can be documented, taught, and transferred from senior to junior designers.</td>
</tr>
</tbody>
</table>
What They Say About ADT

A very powerful tool, makes analog IC design easier and more systematic.

It's more than wonderful. There's no waste of time anymore. Very useful and helpful.
I liked how easy it was to work on ADT.

Great, helpful, very important tool, and very creative idea.
What They Say About ADT

Brilliant and powerful tool. It helps me a lot and saves more effort and time.

An amazing tool that may make a breakthrough in the field.
ADT is like a "Magic Hat" which seems like an ordinary hat, but when the magician puts his hand in it, he gets a rabbit and other things that amaze everyone.

ADT looks very simple with a simple GUI, but when I started to use it, I found many rabbits every time I used it. I was amazed.
ADT: A Paradigm Change!

"If you can't describe what you are doing as a process, you don't know what you're doing."

W. Edwards Deming
So, What’s Next?

- Download ADT NOW and get your free license!
  - adt.master-micro.com
- Start using ADT and send us your feedback!
  - Enhancements, feature requests, etc.!
  - Your feedback really matters!
  - We want to make designers happy 😊

Thank you!
References

References