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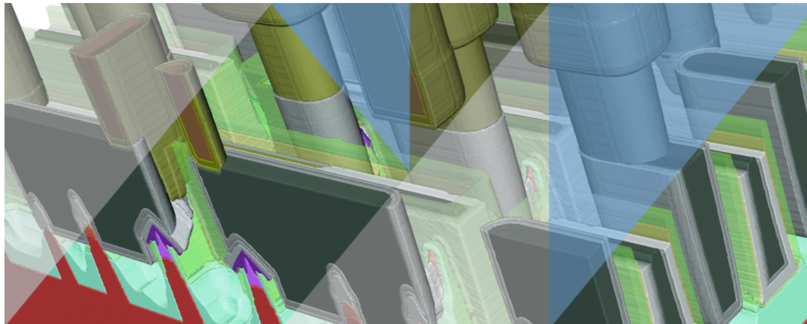
Total Virtual Fabrication of Advanced CMOS Devices and Processing

W. CLARK, ***M. HARGROVE, G. SCHROPFER, D. FRIED – COVENTOR***



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Abstract

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Total Virtual Fabrication of Advanced CMOS Devices and Processing

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Recent advances in semiconductor 3-D device architecture (FinFET, TriGate, embedded memories) and increasingly elaborate process integration flows including High-K/Metal-Gate and multilevel patterning steps have dramatically increased the complexity of integrated circuit processes. The cost and turn-around-time of technology development using traditional trial-and-error experimental methodologies has concurrently increased to the point where it is unsustainable. A more systematic virtual-development approach is required for advanced technologies to tune 3-D device geometry and achieve time-to-market objectives. 3-D process modeling based on a voxel algorithm has already demonstrated its value for MEMS and more recently for semiconductor processing. This capability has been demonstrated in the semiconductor space for a wide range of technology development capabilities in a simple, robust, high-speed software platform. Several examples will be discussed including virtual fabrication, variation analysis and design-process interaction for advanced CMOS flows. Furthermore we demonstrate the interfacing of this virtual design platform to the traditional finite element platforms for the TCAD electrostatic device analysis.

Outline

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- Technology Development Landscape
- Virtual fabrication model methodology
- Case studies
- Summary

Recent Technology Roadmap

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90 — Strained Silicon, Copper Interconnects, 193 nm lithography

65 — 2nd generation strained Silicon, eSiGe, wafer orientation for lo-cost apps

45 — High-K + metal gate, Computational Litho

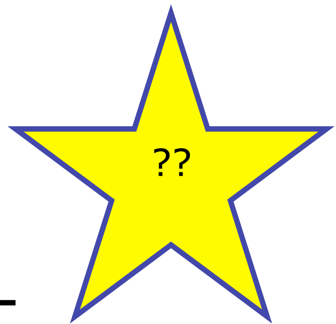
32 — Second generation high-K

Metal
High-k
SiGe
SiGe
Silicon

22 — Ultra-thin body, Fully depleted SOI?

15 — Tri-gate (FinFET), Double Patterning

7 — ???



2002 2004 2006 2008 2010 2012 2014 2016

Semiconductor Process Complexity

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Semiconductor industry trends:

- Entering an era of *performance* scaling, not *geometric* scaling
  - Performance enabled by new materials
  - Performance enabled by new device geometry
- Litho mask count is increasing (from 20 to 45 in last 12 years)
  - Prevalence of LE*^{n}, SAnP, all the EUV precursors
- Process complexity is increasing
  - 500+ steps for Front End of Line
- Unique process flows for Logic, DRAM, Flash
- Technology development costs are increasing
  - 200mm → 300mm → 450nm wafers
- ITRS: Front-End process modeling is a “grand challenge”

- TAT and wafer cost are becoming unsubstainable

Virtual modeling objectives

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- Predictability
- Robustness
- Efficient in time/storage
- One path to achieve these objectives –
  - Model the outputs rather than the inputs
  - Behavioral model rather than first principal (Reactor-scale)
  - Provide a basic set of process models for non-critical areas
    - Etch, Deposit/growth, Photolithography, planarization
  - Provide a more detailed process suite for critical areas
  - Provide ‘fab-like’ virtual metrology suite of tools for direct measure of output
  - Provide ability to perform batch-jobs

More complex processes

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- Multi etch
  - Etch multiple layers with provision for
    - Sputtering, sidewall copolymer deposition, taper etc
- Silicon directional etch – along major crystal directions
- CMP planarization
  - Overpolish regimes and dishing
- Visibility deposition
  - Snowfall like depositions
- Epi growth with plane variability
- Pattern dependent etching
  - Isolated and nested feature distinctions

SEMulator3D 2014
Automation – Virtual Metrology

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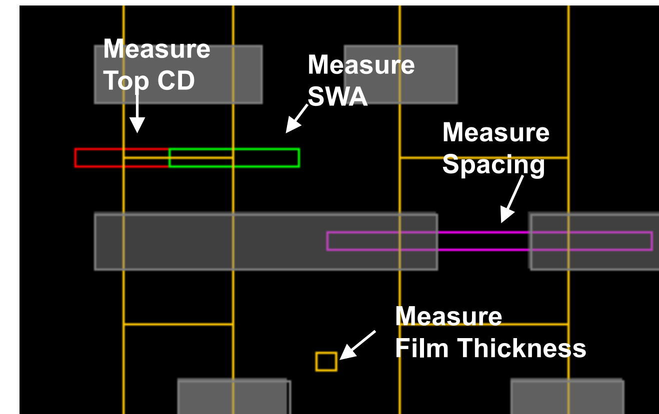
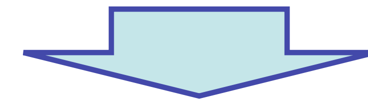
- Automate in-line, local measurements of critical technology parameters.
- Mimic real in-fab metrology, replace slow out-of-fab destructive characterization.

Specify Measurement Regions

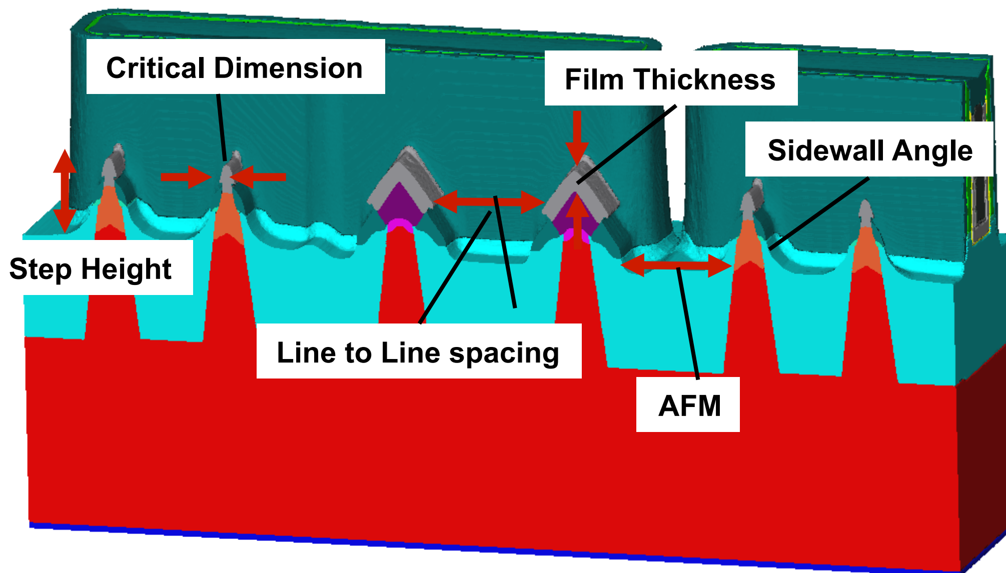




Get Numerical Metrology Results

```
M1_DCD = 29.1000469068
M1_DCD_LE = 36.8996629246
M1_MO_CD = 33.3335230507
M1_MOCD_LE = 32.3436509895
M1_FCD = 41.0305322702
M1_FCD_LE = 24.9009646571
M1_Cu_Area = 2273.078125
M1_Area = 3914.4375
M2_L1_DCD = 29.1
M2_E1_HMO_CD = 31.6147704591
M2_L2_DCD = 29.1000312598
M2_E2_HMO_CD = 31.6147704591
M2_HMO_E1E2_Space = 32.3935856442
TiN_PostHMO = 15.0
V1_Y_DCD = 29.100023443
TiN_PostViaPartial = 12.0
```

Virtual Metrology Measurement Options



What is SEMulator3D?

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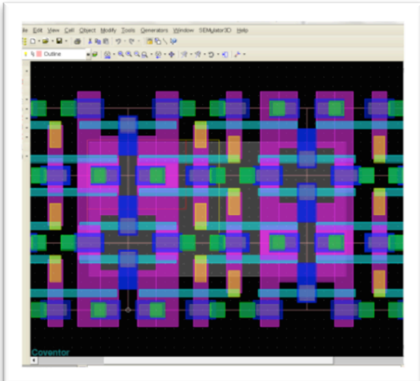
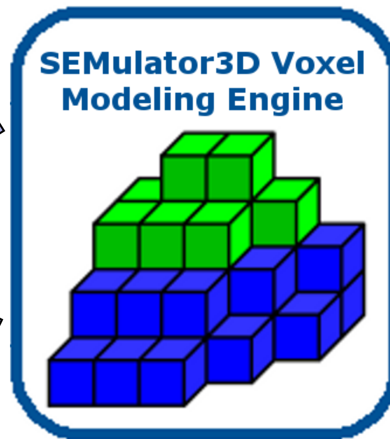
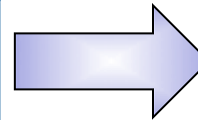
A Powerful 3D Semiconductor Modeling Platform



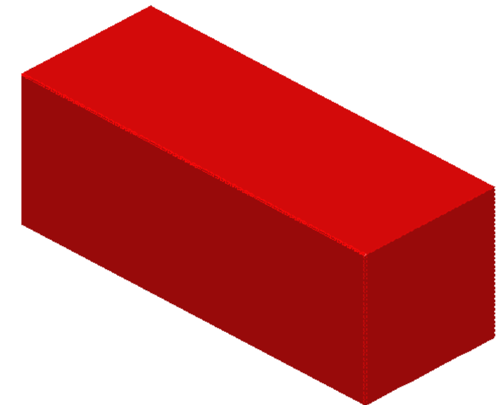
Layout Editor:
Design, OPC, PrintSim, etc.





Process Editor:
Step-by-Step Process
Behavioral Description

3D Viewer:
RMG FinFET Demo
Self-Aligned Contact
TFMHM BEOL w/ SAV



- Applicable to ANY process & ANY layout
- Replaces build & test with **accurate** 3D modeling of large areas & complex process sequences
- Provides validation and visualization of relationships between design and process
- Provides a **predictive** view of design-technology interactions

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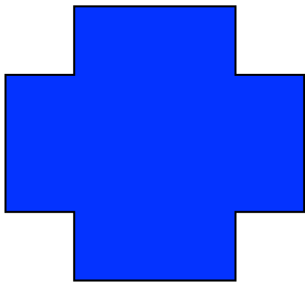
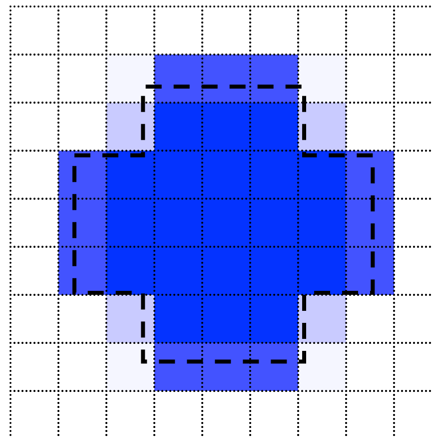
SEMulator3D is primarily a ***voxel*** modeling tool.

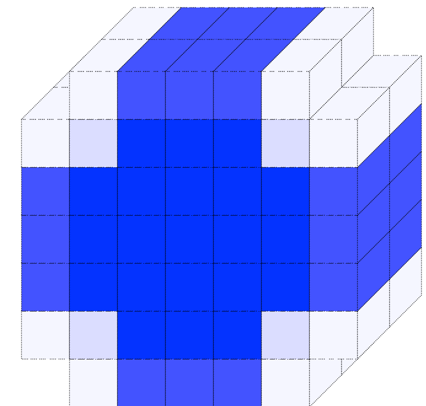
Voxels are like 3D pixels:



A 2D shape



The same 2D object, represented with pixels. Note the partly filled pixels!



A similar 3D shape, represented with voxels. The color represents the ***volume fraction****.*

SEMulator3D voxels can be partly filled, just like pixels.

Voxel Size and Performance

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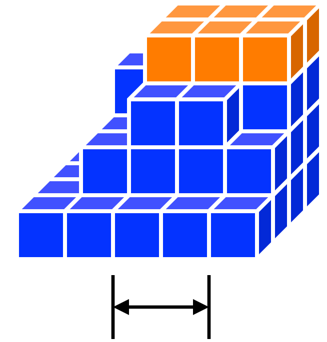
SEMulator3D uses patented voxel modeling algorithms:

- Data compression exploits self-similarity in the model to reduce memory use.
  - Compression ratios of 10,000:1 (vs. storing all voxels) are not uncommon
  - Particularly efficient for semiconductor processes
- Acceleration algorithms also exploit self-similarity in the model to greatly reduce the time required to build models.



Guideline:
At least 2 voxels across the smallest model feature.

BUT – voxel size has a large impact on performance.

- In SEMulator3D, voxel size is called “Model Resolution” and can be chosen by the user.
- Lower resolution to save compute time and memory.
- Higher resolution to resolve small details.

Case Studies

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1. Virtual Process window study
2. Electrostatic response analysis to FinFET profile variability

1) SISPAD 2013
2) DAC 2014

Case study 1 – process window

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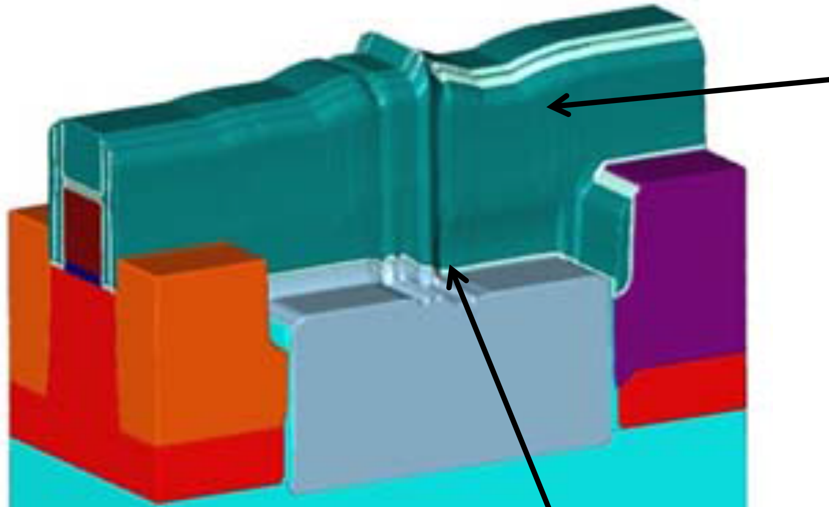

cap nitride remain thick enough to protect the gate silicon during the dual-epitaxial source/drain modules, but must also be thin enough to ensure complete top-removal for uniform silicide formation

pfet

nfet

Gate transition over n-p boundary compounded by multiple generated mask edges during spacer and trench etches

Case study 1 – model calibration

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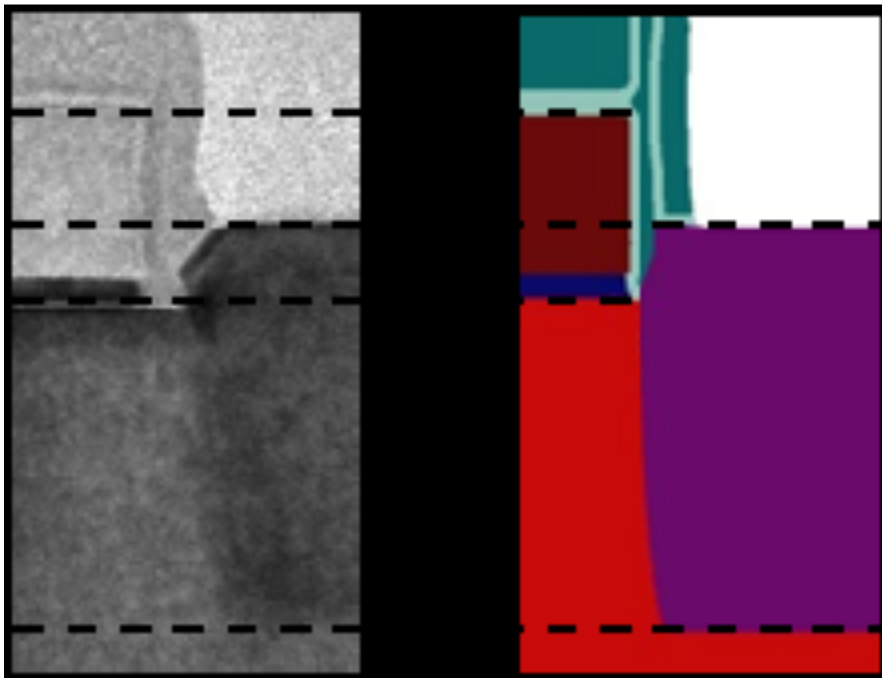
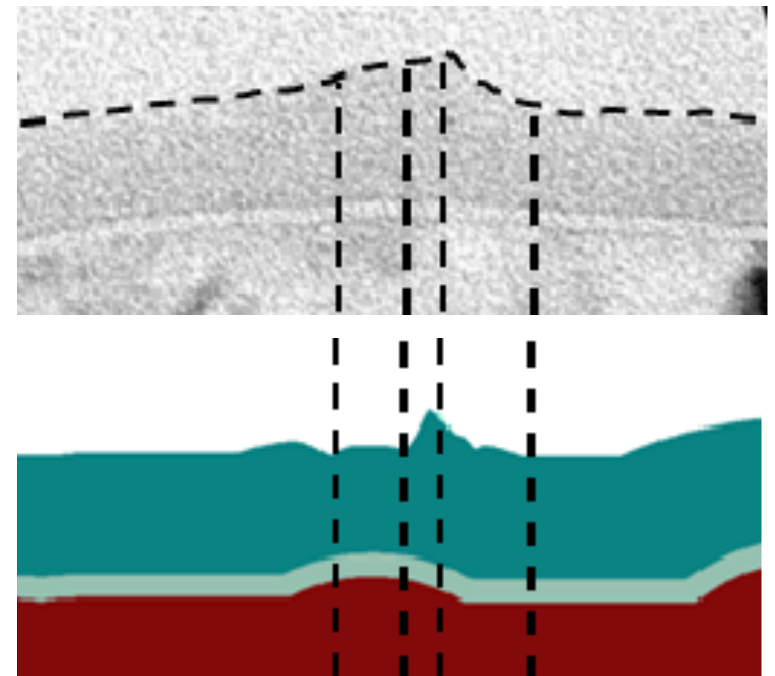
Model calibration to inline physical measurements

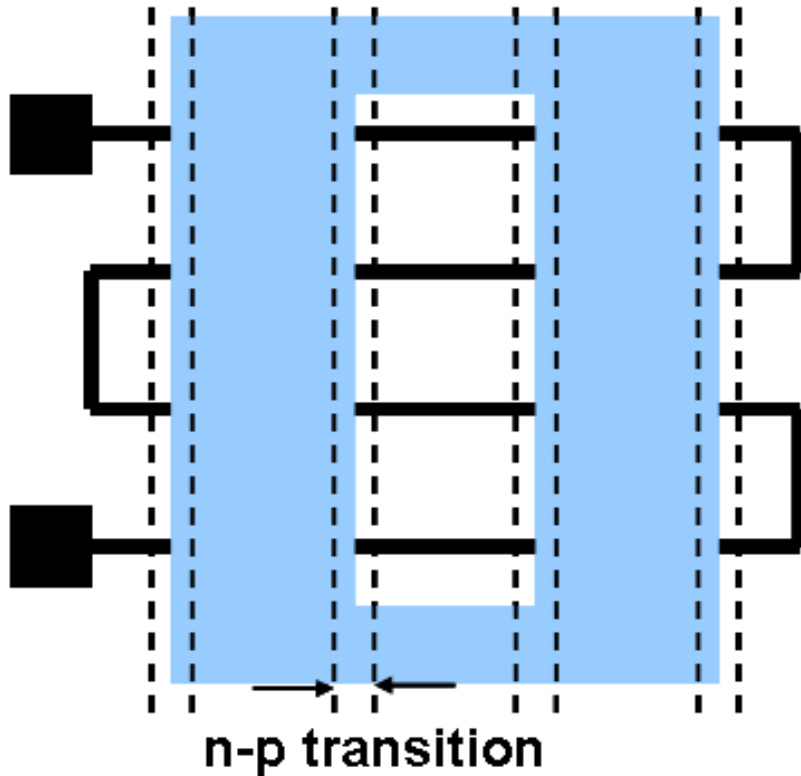


Cross gate section

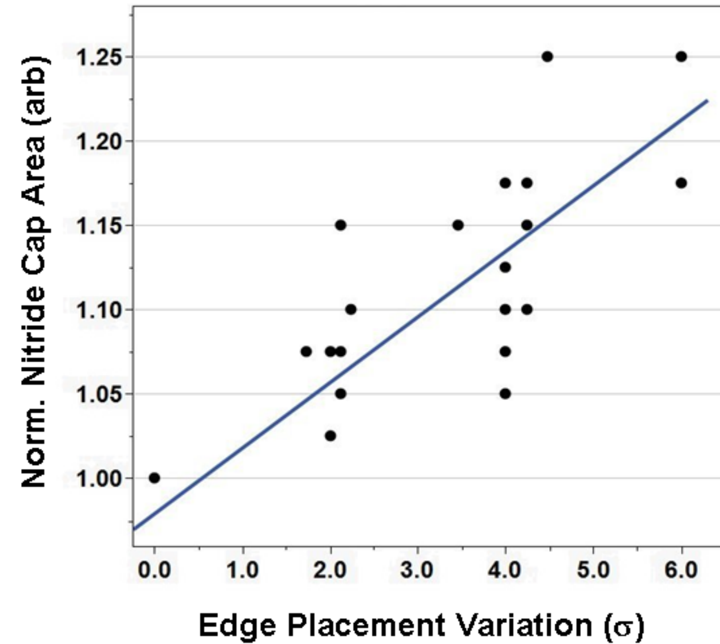


Through gate section

Case study 1 – create test structure and determine response



Enhanced response structure



Integration of calibrated virtual nitride profiles vs Edge placement variation

Case study 1 – characterize test structure

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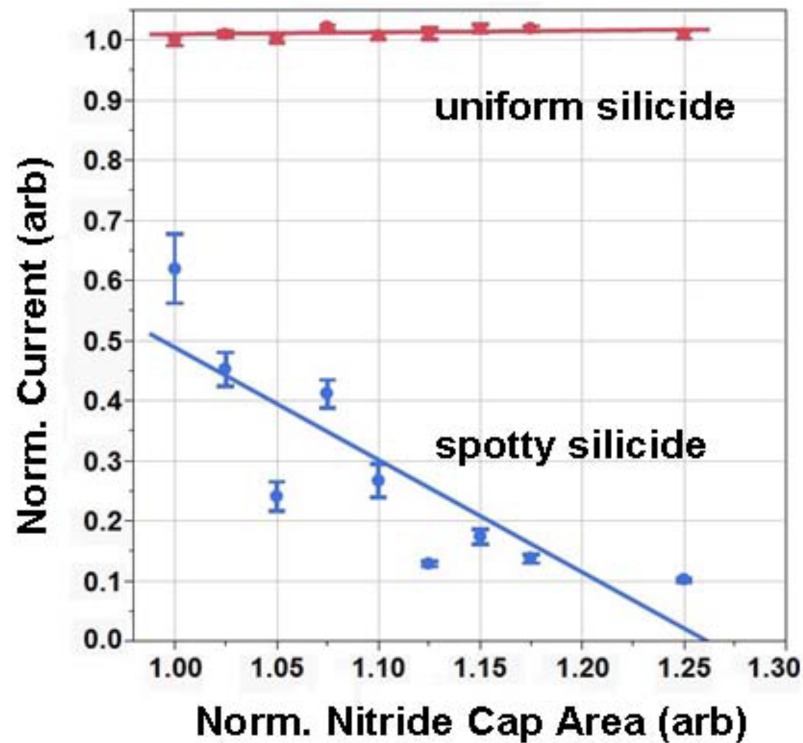
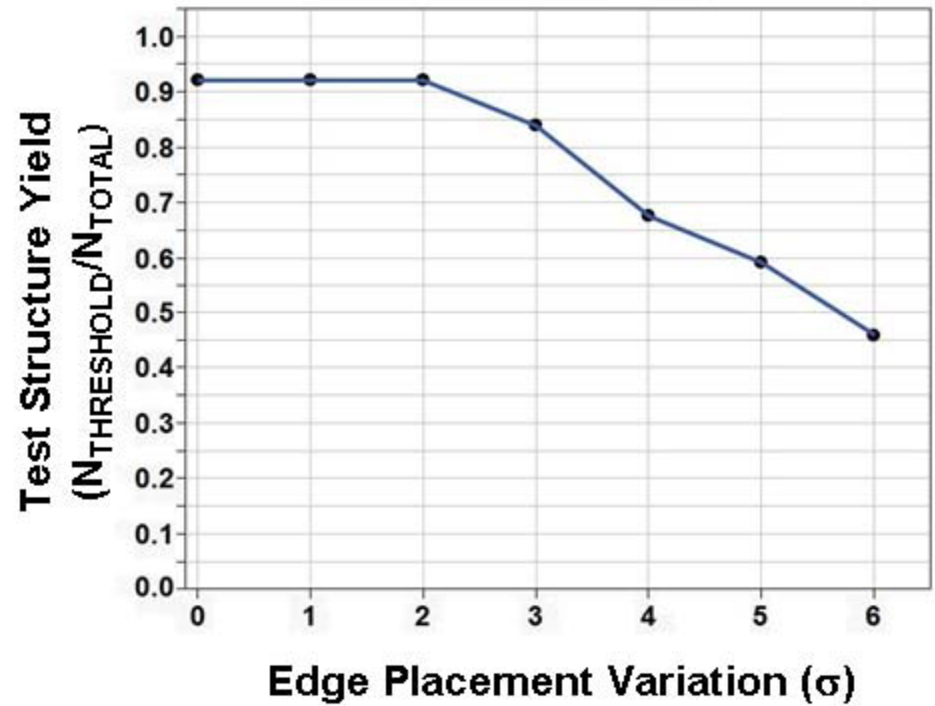


Sensitivity to Edge placement variation



Sensitivity to Edge placement variation

Case study 1 – optimize profiles

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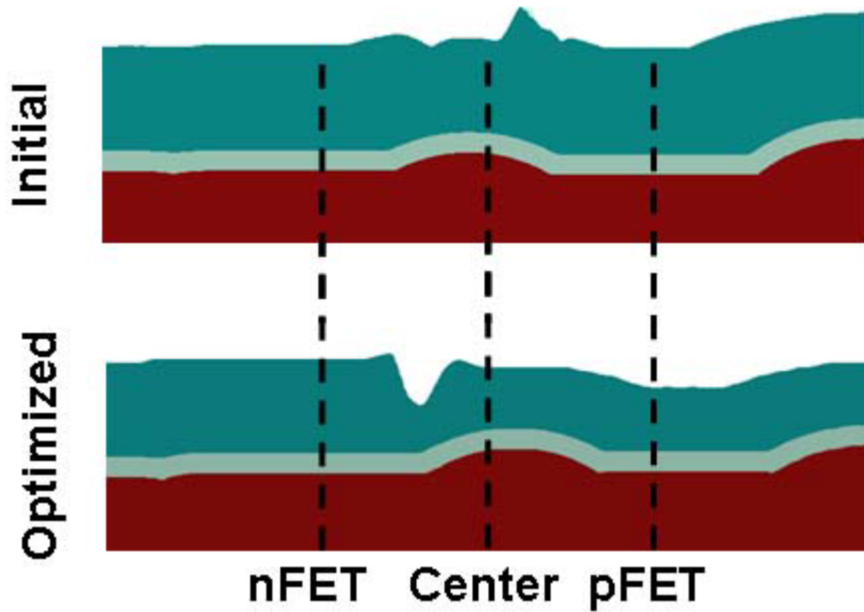
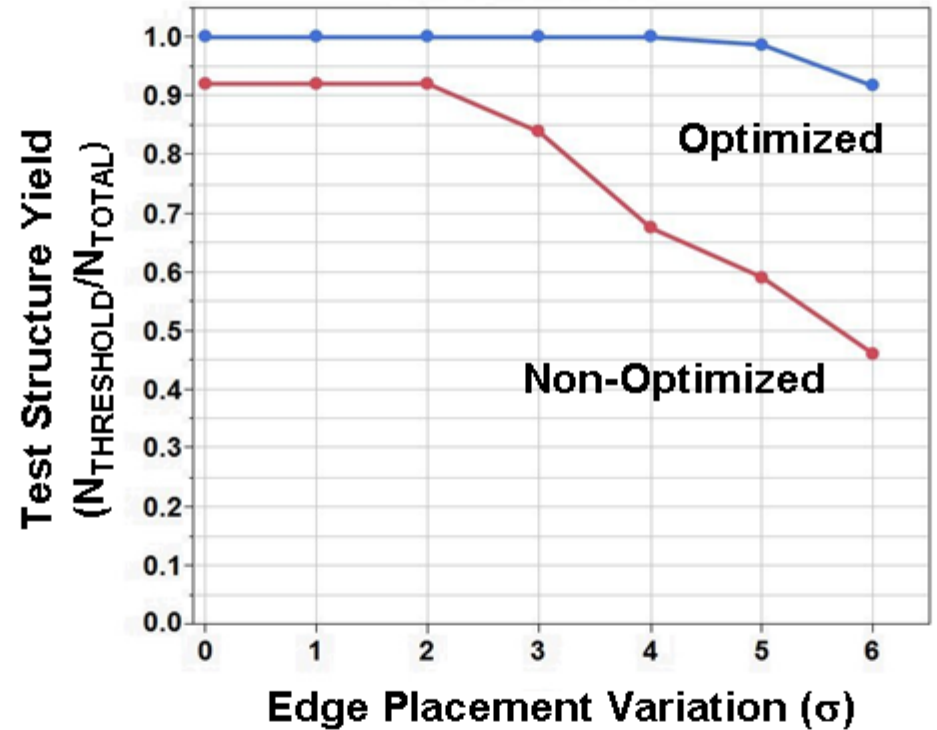


Resist profile initial vs model optimized



Optimized response curve

NET: Process window extended from 2σ to 5σ

Case study 2 – Electrostatic response to Fin profile variation

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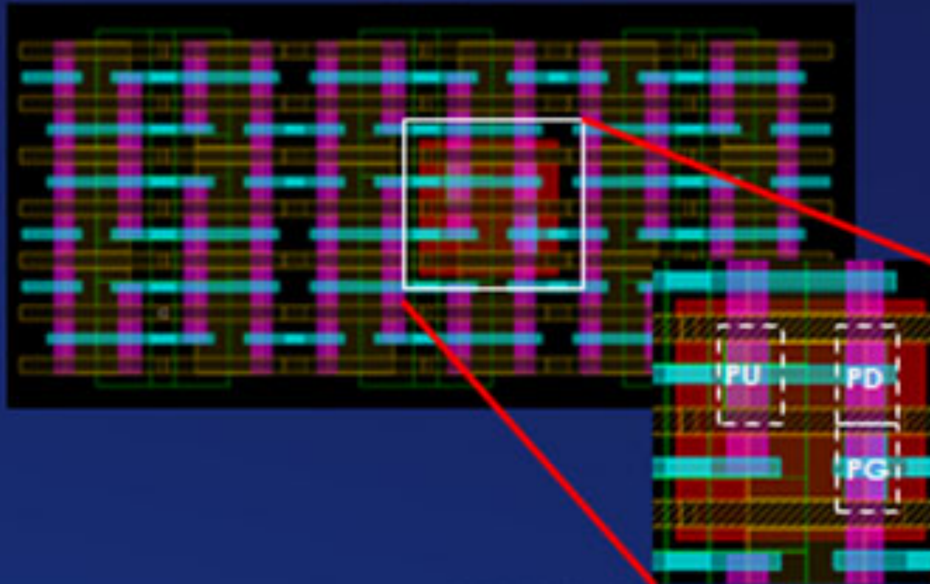
- Virtual model build of FinFET
  - Using standard 6-T SRAM cell
  - Conventional Graphics input
- Virtual DOE around Fin nominal parameters
  - Depth (100nm), Fin angle (7°)
  - STI recess etch (30nm)
- Apply appropriate meshing
- Output to TCAD system

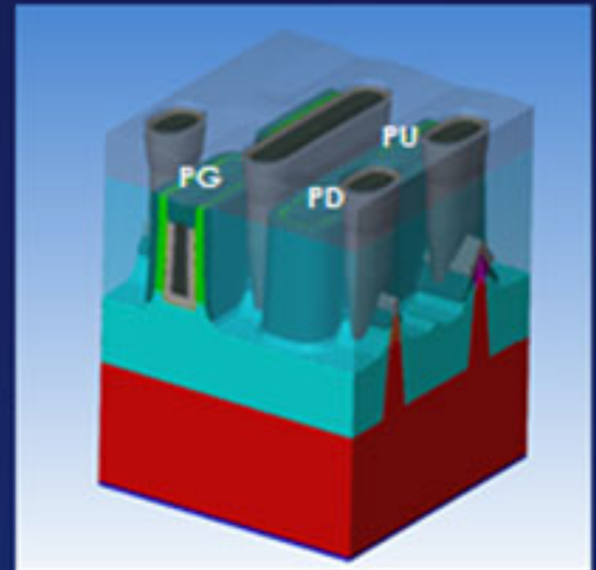
Case study 2 – Fly cell model build

Mask Layout Input
Full 16nm FinFET SRAM



SRAM Half Cell Extracted for Model Build

SRAM Half Cell Built in SEMulator3D
Based on complete 16nm Process Flow



Case study 3 – Fin profile

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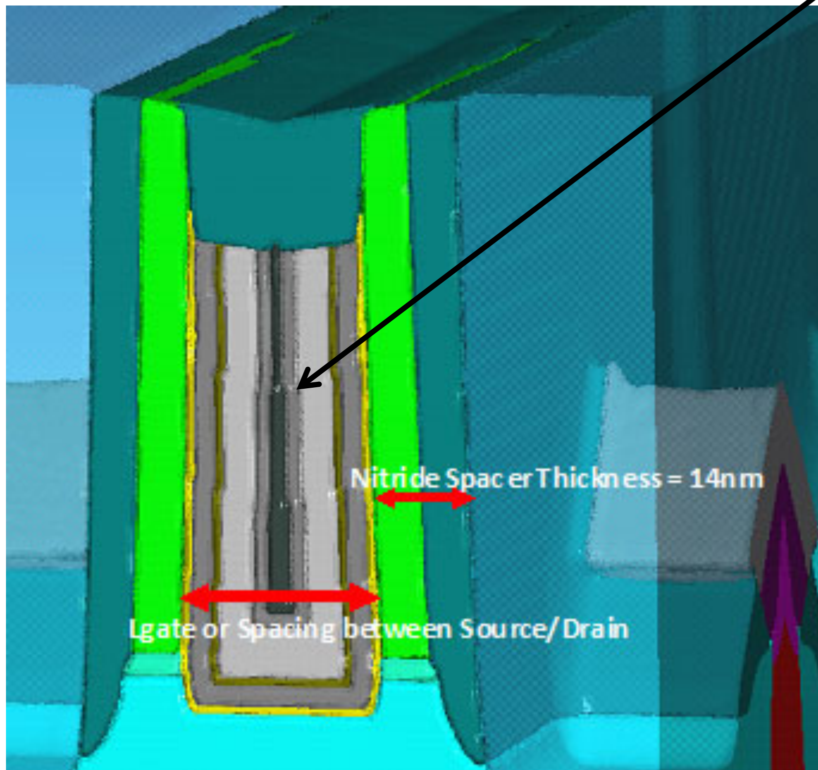

The final replacement metal gate (RMG) device cross-section is accurately modeled by a calibrated set of high-k parameter values that realistically represent existing published data.

Case study 2 – Large area mesh to TCAD

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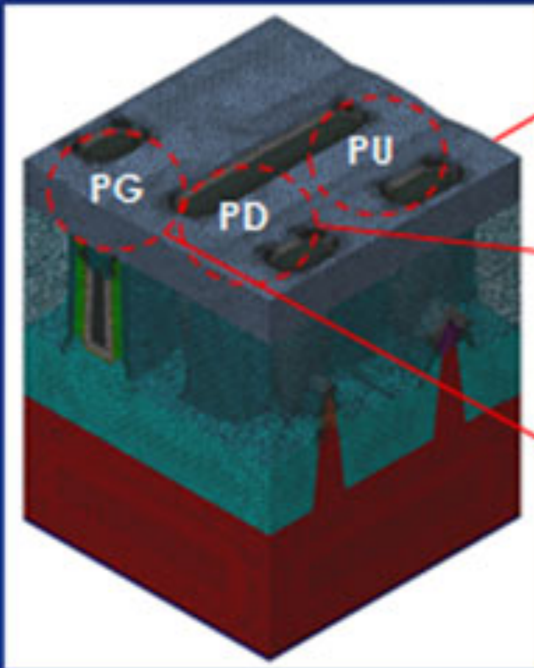
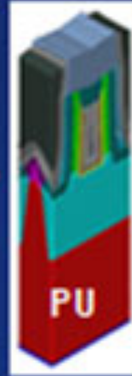
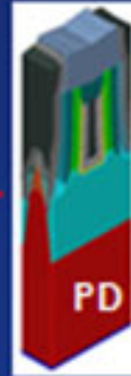
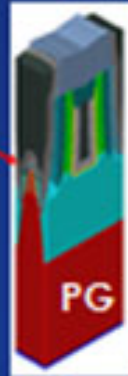
Export Large Area Mesh



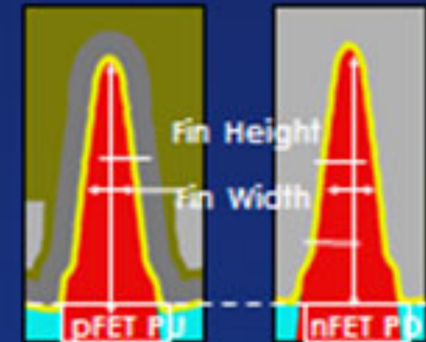


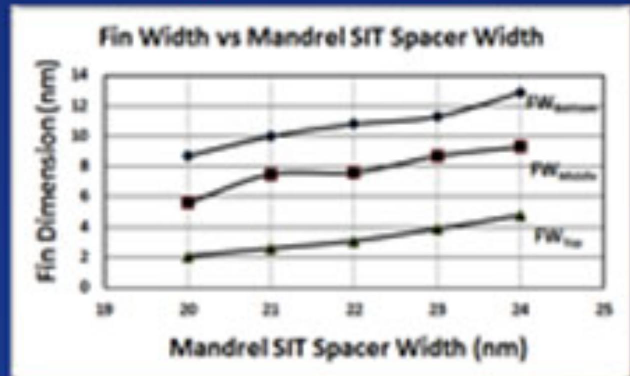




Crop Individual Devices

SEMulator3D Expeditor Variation Study of Fin Profile





Case study 2 – Device Simulation

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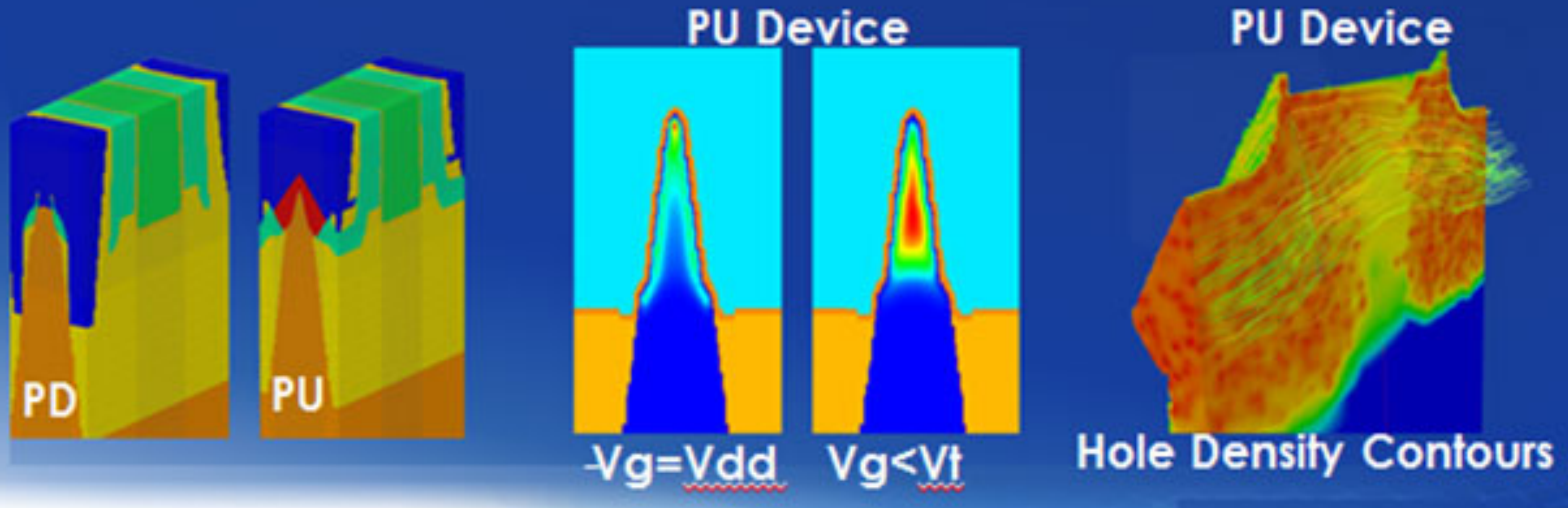

Hole density profile response to bias condition - key to optimizing performance

3D hole-density contour plot through the middle of the channel from source-to-drain
Note discrete impurity atoms in Fin.

Summary

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- Virtual fabrication methodology enables significant yield predictability verified by product results
- Ability to provide predictable process simulations and to emulate fab measurements is key
- Virtual fabrication methodology provides predictable structural variations for electrostatic analysis engines