Performance comparison of Hall Effect Sensors obtained by regular bulk or SOI CMOS technology

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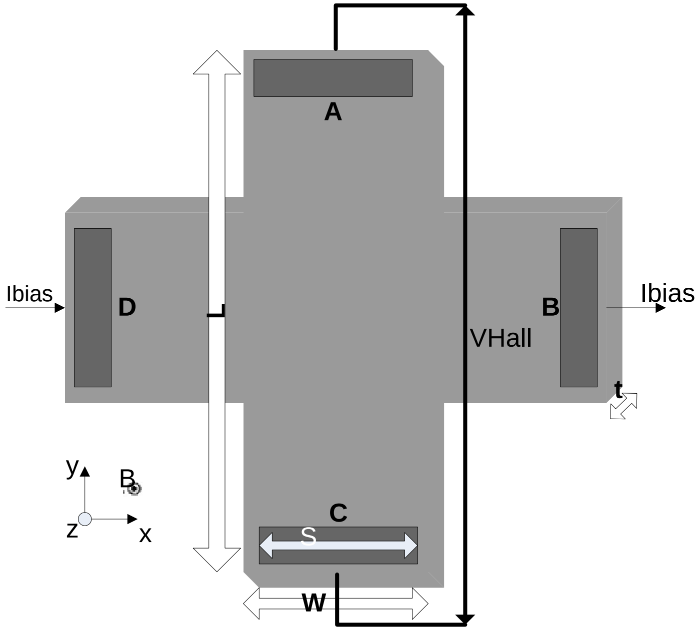
OUTLINE

- Different Hall cells have been integrated in both bulk and SOI CMOS technology and analyzed in terms of their specific parameters.
- The first one is XFAB regular bulk CMOS XH 0.35 µm and the second one is XFAB SOI XI10 1 µm non-fully depleted.
- Geometry plays an important role in Hall cells performance. The focus of this work is on the XL Hall cell.
- The most important parameters of a specific Hall cell, based on both regular bulk and SOI structures, are evaluated through three-dimensional physical simulations.

Hall Effect Sensors



(1) $$\boxed{V_{HALL} = S_A B}$$

$$\boxed{S_A = \frac{Gr_H}{nqt} I_{bias}}$$ (2)

- low-power applications
- current sensing
- position detection & contactless switching

Hall Cells Design Selection

- Different 3D Hall sensors were integrated in both regular bulk and SOI CMOS.
- They are all symmetrical and orthogonal structures.
- The geometry plays an important role in the sensors performance.

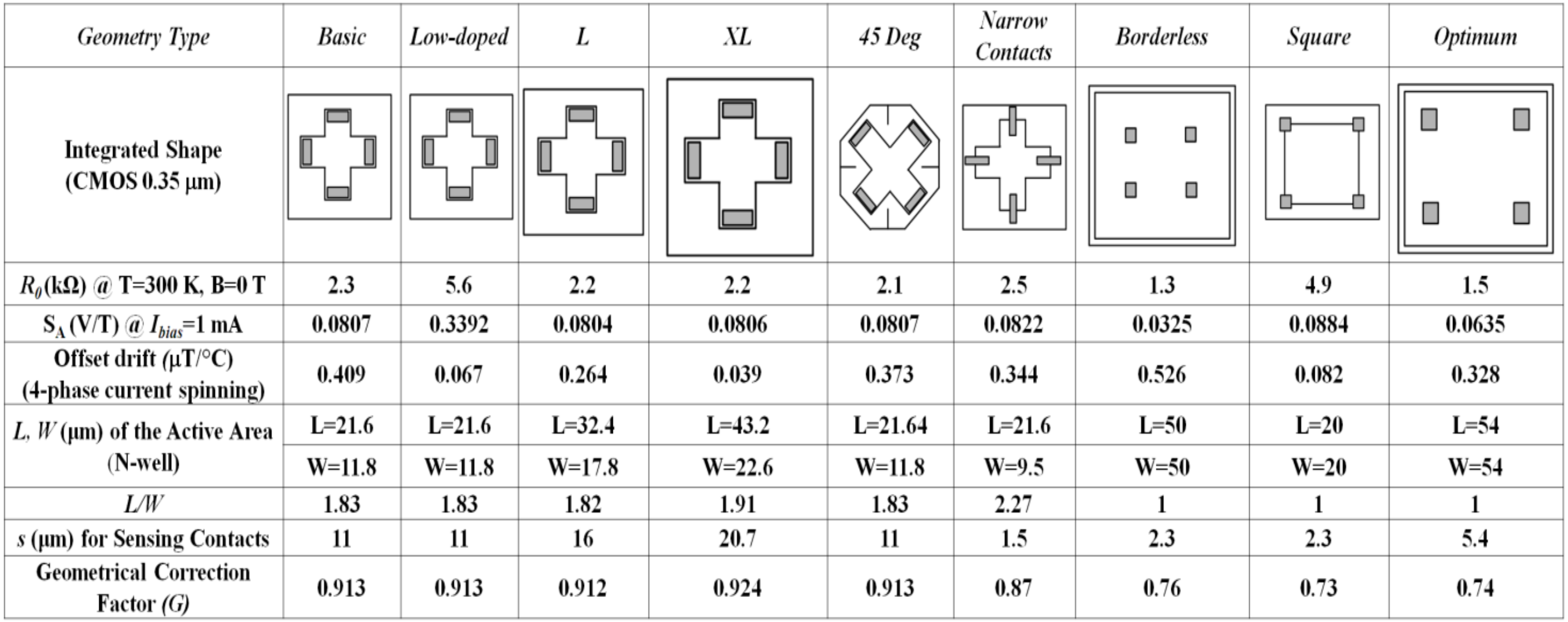
$$\boxed{G \cong 1 - \frac{16}{\pi^2}\exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\left[1 - \frac{8}{9}\exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\right]\left(1 - \frac{\theta_H^2}{3}\right)} \qquad (3)$$

valid if $0.85 \le L/W < \infty$ and $0 \le \theta_H \le 0.45$

Hall Effect Sensors Measurements

- Measurements results on nine different Hall Effect sensors in regular bulk CMOS
- Similar results expected soon for the SOI counterparts

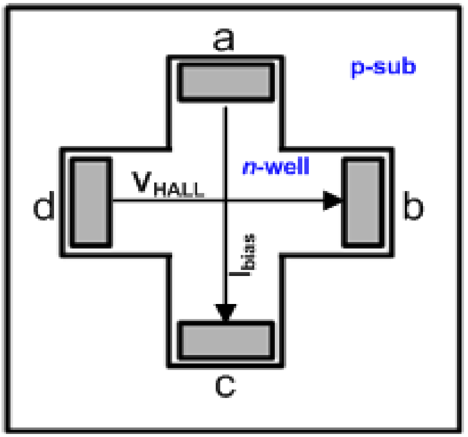
Objectives: offset @ T=300 K **< ±30 µT** & *offset drift* < **±0.3 µT/°C**



Geometry Type	*Basic*	*Low-doped*	*L*	*XL*	*45 Deg*	*Narrow Contacts*	*Borderless*	*Square*	*Optimum*
Integrated Shape (CMOS 0.35 µm)									
R_0(kΩ) @ T=300 K, B=0 T	2.3	5.6	2.2	2.2	2.1	2.5	1.3	4.9	1.5
S_A (V/T) @ I_{bias}=1 mA	0.0807	0.3392	0.0804	0.0806	0.0807	0.0822	0.0325	0.0884	0.0635
Offset drift (µT/°C) (4-phase current spinning)	0.409	0.067	0.264	0.039	0.373	0.344	0.526	0.082	0.328
L, *W* (µm) of the Active Area (N-well)	L=21.6	L=21.6	L=32.4	L=43.2	L=21.64	L=21.6	L=50	L=20	L=54
	W=11.8	W=11.8	W=17.8	W=22.6	W=11.8	W=9.5	W=50	W=20	W=54
L/W	1.83	1.83	1.82	1.91	1.83	2.27	1	1	1
s (µm) for Sensing Contacts	11	11	16	20.7	11	1.5	2.3	2.3	5.4
Geometrical Correction Factor (*G*)	0.913	0.913	0.912	0.924	0.913	0.87	0.76	0.73	0.74

Single Phase and Residual Offset

- Cell polarization and the corresponding phases



Greek-cross cell polarization

Phases	Ibias	V_{HALL}
Phase 1	**a to c**	**b to d**
Phase 2	**d to b**	**a to c**
Phase 3	**c to a**	**d to b**
Phase 4	**b to d**	**c to a**

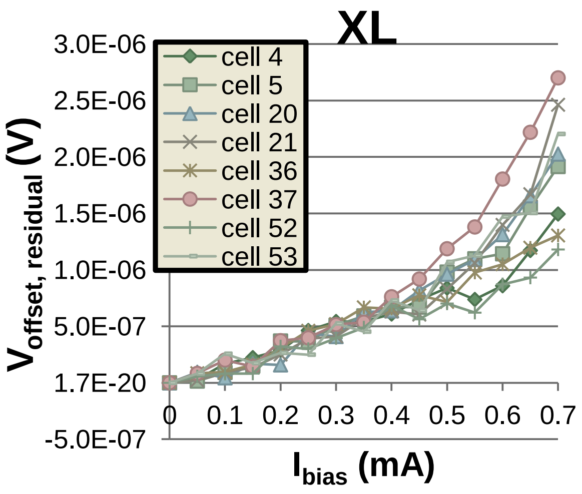
- Single phase offset and residual offset

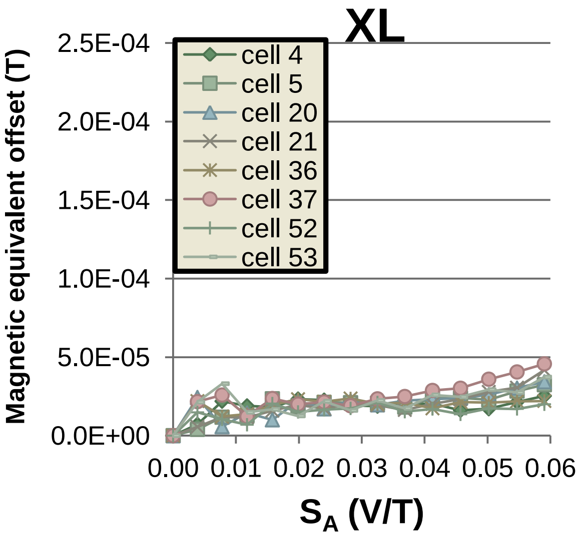
$$\boxed{V_{out} = V_{HALL}(B) + V_{offset}} \qquad (4)$$

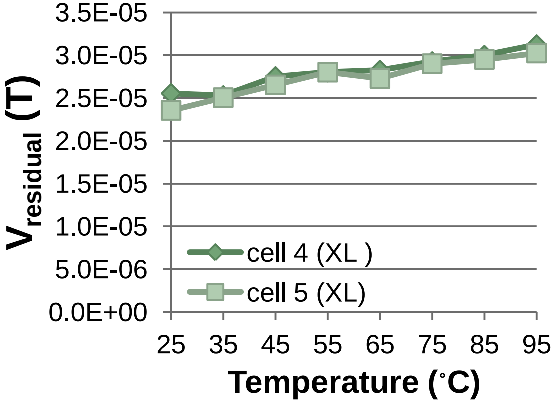
$$\boxed{Offset_{residual\ (4\ phase)} = \frac{V_{P1} - V_{P2} + V_{P3} - V_{P4}}{4}} \qquad (5)$$

Offset measurements

- Measured for XL regular bulk CMOS, results expected soon for XL SOI







Regular bulk vs. SOI CMOS technology

The sensors fabricated in SOI (***S***ilicon ***O***n ***I***nsulator) technology have obvious benefits, with respect to the bulk Hall sensors.

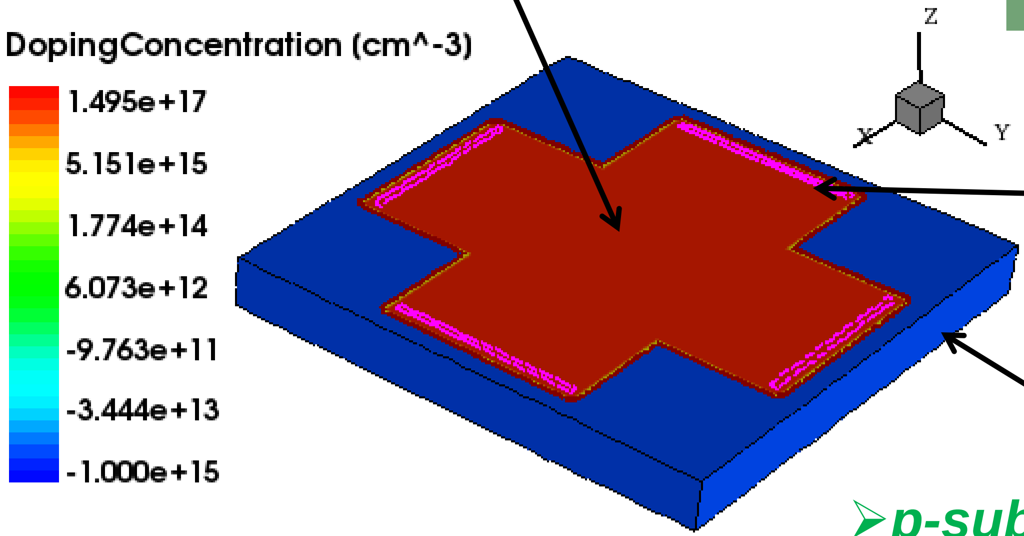
- higher magnetic sensitivity
- less noise generation
- possibility to use lower biasing voltage
- smaller leakage current through the dielectric
- enhanced radiation resistance etc.

The 3D Simulation of regular bulk Hall Cells

- **The XL structure follows the XFAB XH 0.35 fabrication process.**

Parameter	Value
L (µm)	43.2
W (µm)	19
Contacts dimension s (µm)	18.3

- ***active n-well region:*** **Arsenic doping**
  - ✓ **Gauss profile implantation**
  - ✓ **1.5*10^{+17} cm^{-3}**



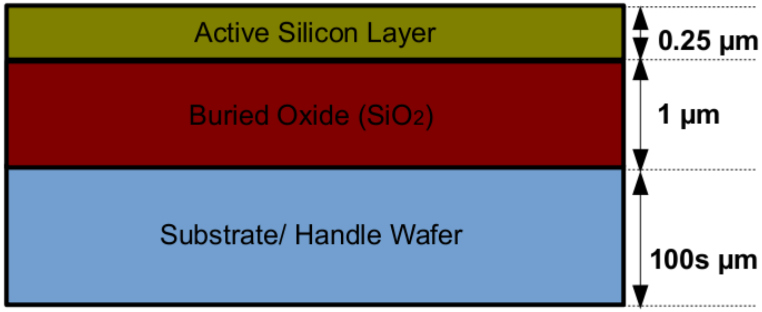
- ***electrical contacts***

- ***p-substrate:*** **Boron doping concentration of 10^{+15} cm^{-3}**

The 3D model of XL regular bulk Hall cell

SOI CMOS technology

➢ The stacking of the layers, according to a SOI XFAB XI10 fabrication process.



➢The active silicon layer is found on top of the dielectric buried silicon oxide (SiO_2) layer, which is in its turn found on the silicon substrate, or handle wafer.

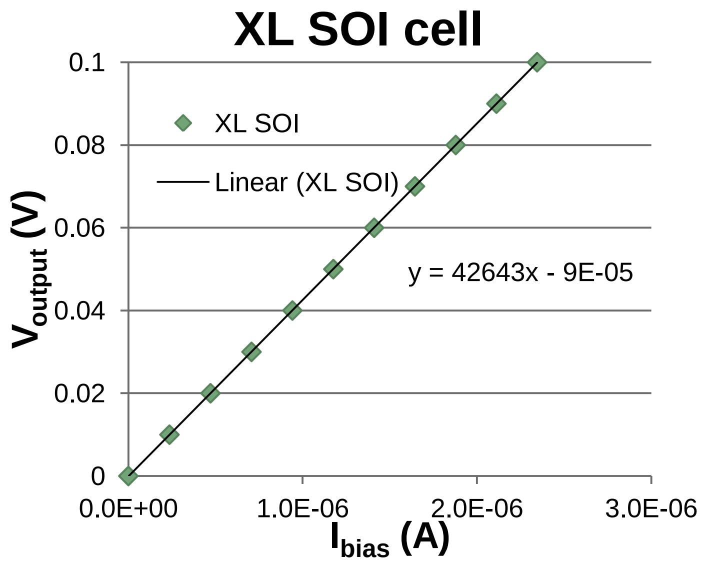
DOPING CONCENTRATIONS IN THE SOI HALL CELL FABRICATION

Layer	Type	Numerical value
Wafer (handle) substrate	Si, p-doped (Boron)	6.5 E+14 cm^{-3}
Dielectric	Buried Silicon Oxide, $Si0_2$	
p-substrate in active Silicon layer	Si, p-doped (Boron)	1E+15 cm^{-3}
n-well in active Silicon layer	Si, n-doped (Arsenic)	5E+16 cm^{-3}

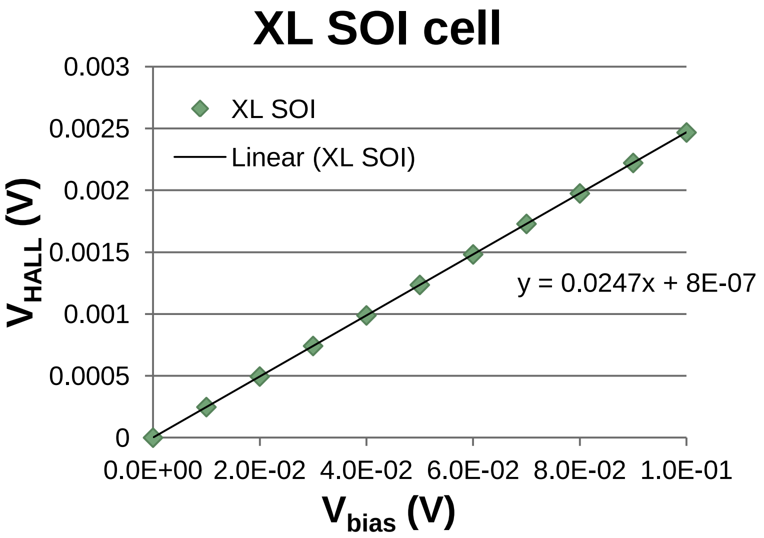
3D Simulations results (II)

SOI XL cell:

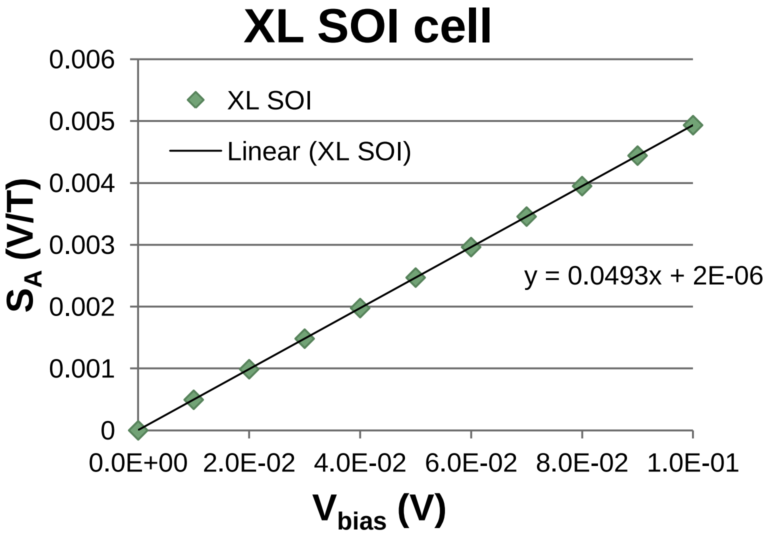
- I-V characteristics
- V_{HALL} estimation
- Sensitivity numerical estimation



V-I characteristics, SOI XL, R_{input}=42 kΩ



Hall voltage vs. biasing voltage, SOI XL

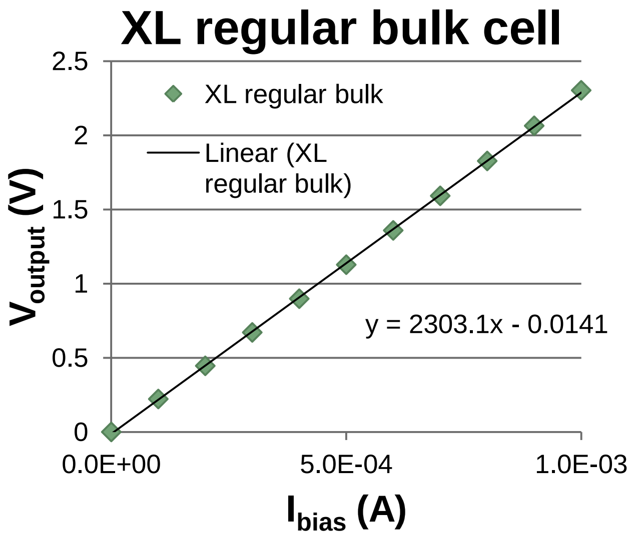


Sensitivity vs. biasing voltage, SOI XL

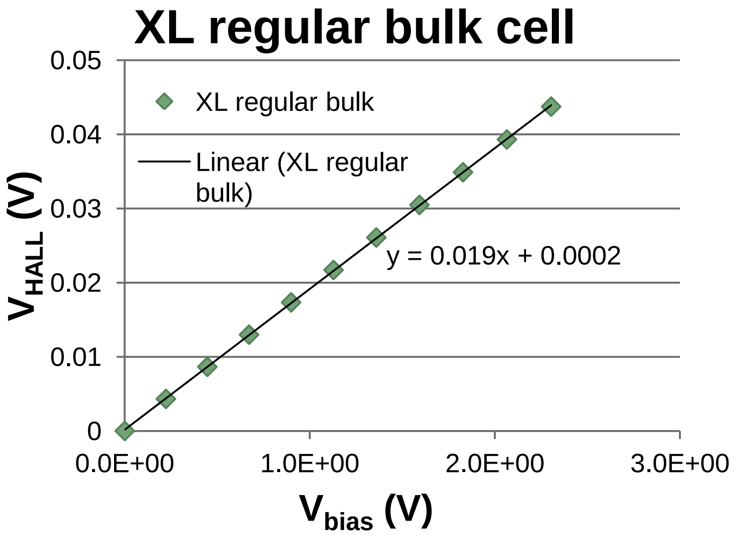
3D Simulations results (III)

Regular bulk XL:

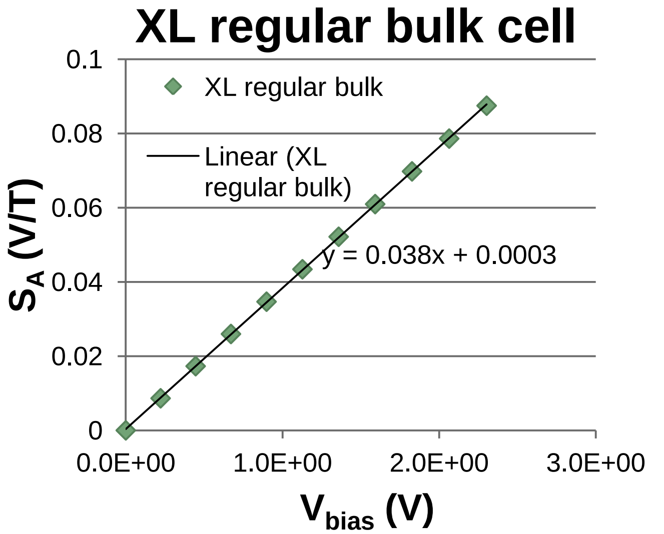
- I-V characteristics
- V_{HALL} estimation
- Sensitivity numerical estimation



V-I characteristics, regular bulk XL, R_{input}=2.2 kΩ



V_{Hall} vs. biasing voltage, regular bulk XL



S_A vs. biasing voltage, regular bulk XL

Conclusions

- This work was intended to analyze the behaviour of the XL Hall cell in both regular bulk and SOI CMOS fabrication process, by performing three-dimensional physical simulations.

- The Hall voltage, absolute sensitivity and input resistance were extracted through simulations.

- With respect to equivalent devices fabricated in regular bulk, the Hall devices built in SOI technology offer higher absolute sensitivity.

References (selective list)

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Thank you for your attention!