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Compact Model of Tunneling Field Effect Transistor for Ultra-low Voltage Circuit Analysis

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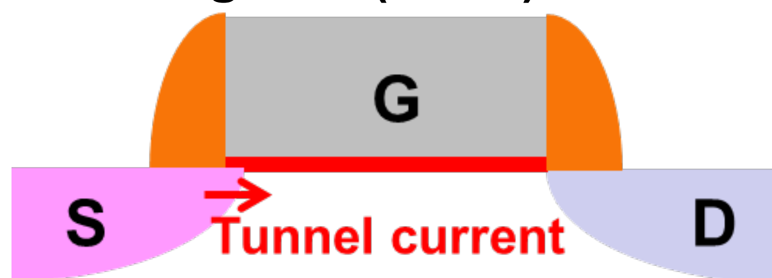
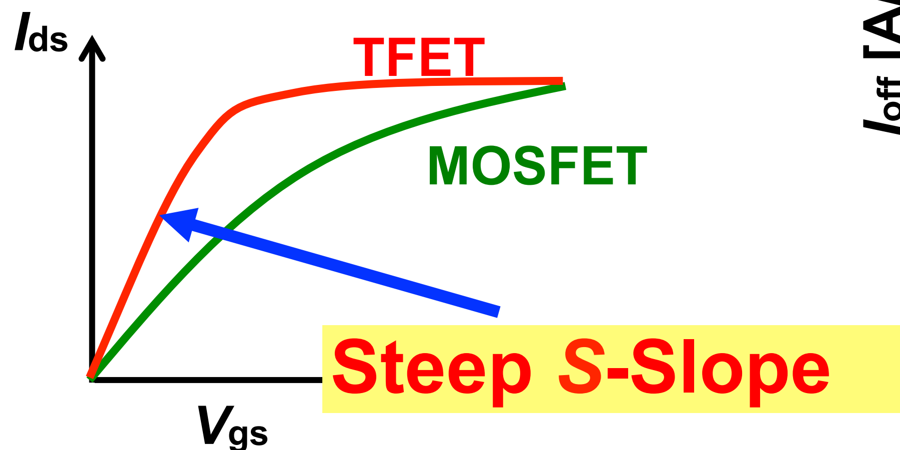
Outline

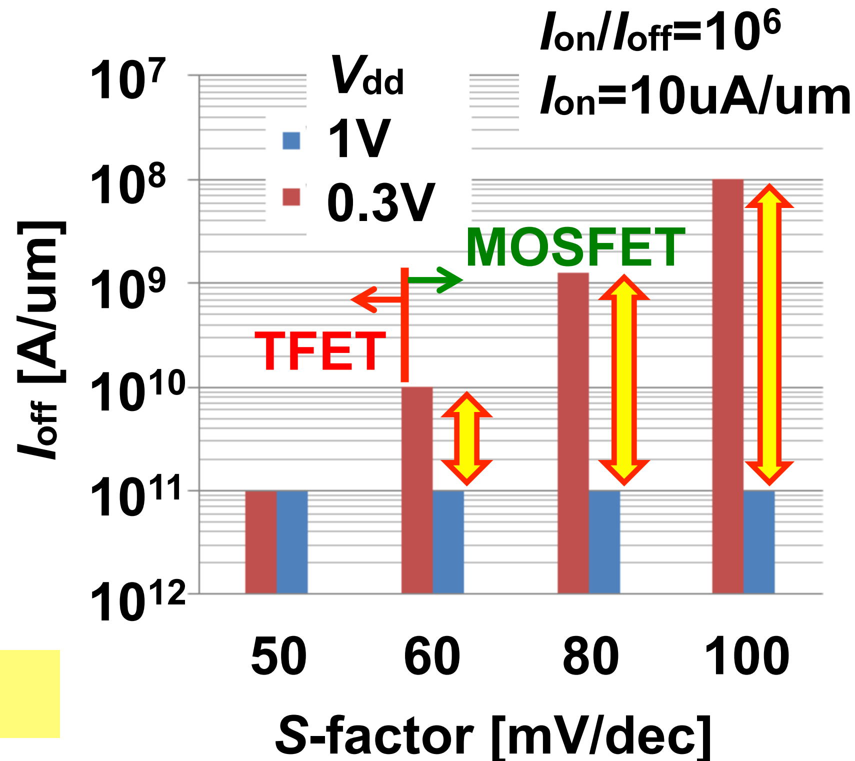
1. Introduction
2. TFET model concept
3. Model evaluation
   and Circuit simulation results
5. Summary

Introduction: TFET – device feature and circuit application

Tunneling FET (TFET)





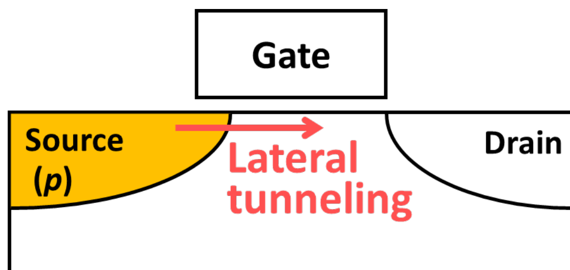


Fast switching and low power!

1st issue: performance optimization for various device structure of TFET

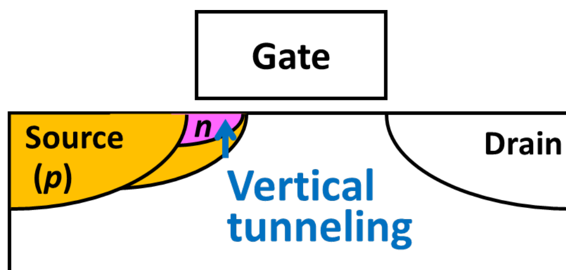
So high tunneling probability and high electron density are needed,

conventional



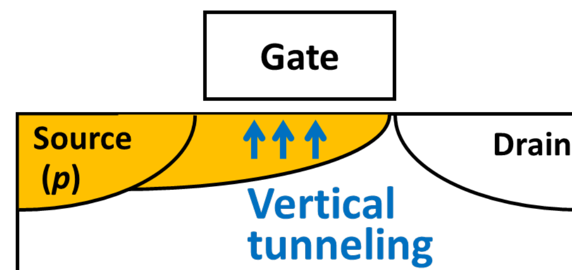
Simple process
Low I_{on}

g-FET (Berkeley)

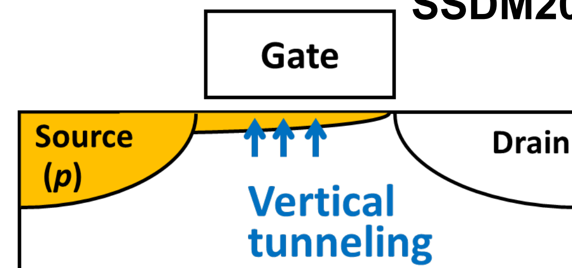


Simple process
Low I_{on}

SJL-TFET (Toshiba)
SSDM2014



Btm.S-TEFT(Toshiba)
SSDM2014

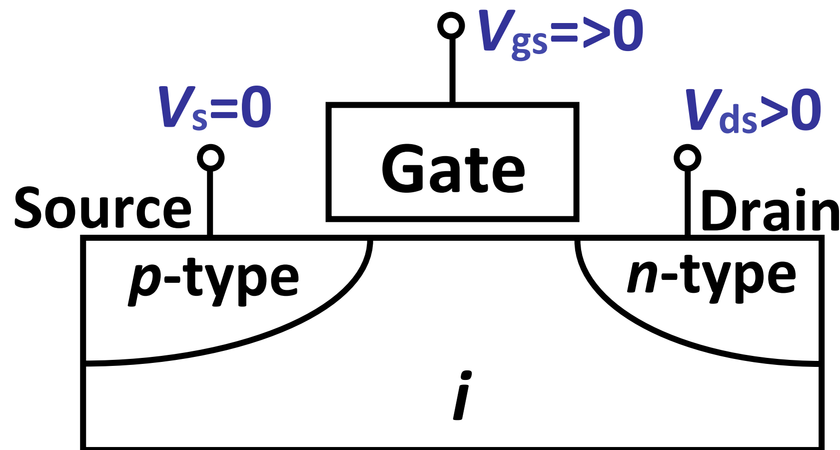


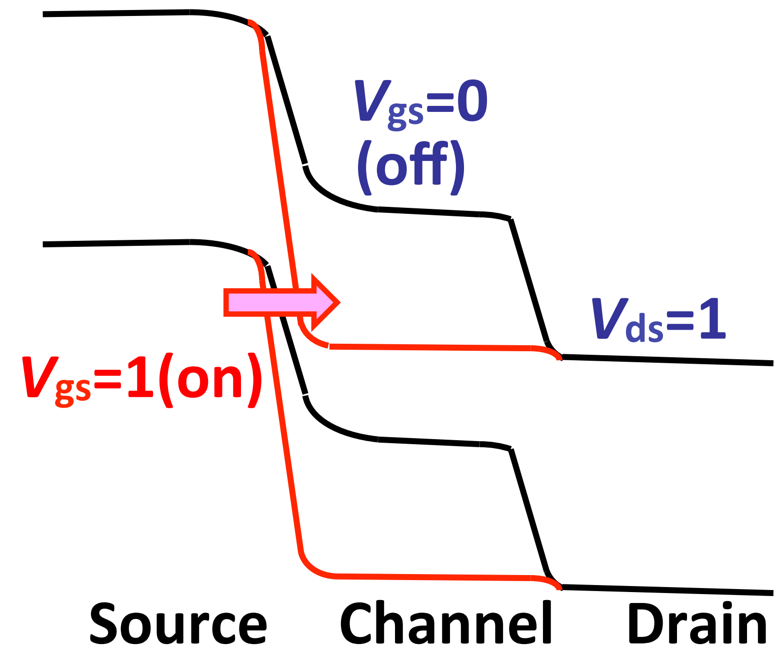
High I_{on}
Low variability

The critical device parameters for each TFET are different!

2nd Issue: For the circuit simulation, I_{ds} under the various V_{gs} and V_{ds} conditions are needed!

Switching operation for *n*-type TFET





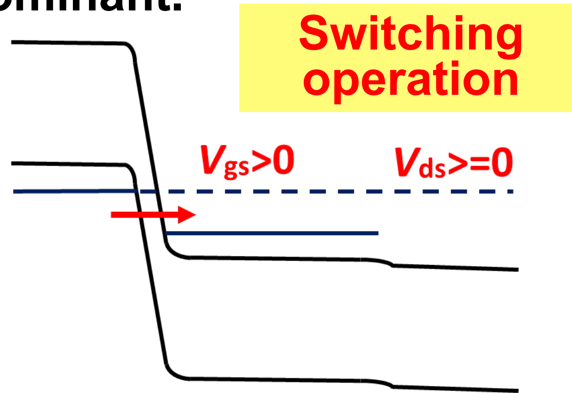
Reverse bias condition for *p*-*n* junction

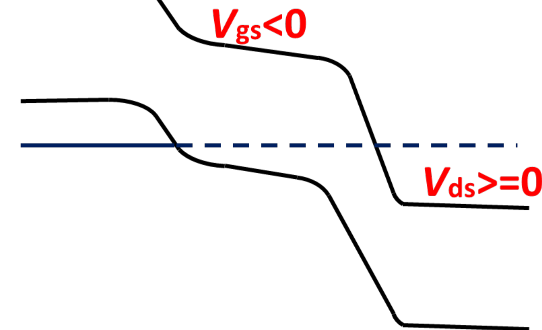
TFET operation under the various bias conditions

(1) S-D reverse bias conditions (V_{ds}>=0)

(a) V_{gs}>0: BTB tunneling current is dominant.

(b) V_{gs}=<0: TFET is in the off state. I_g and I_j should be considered.

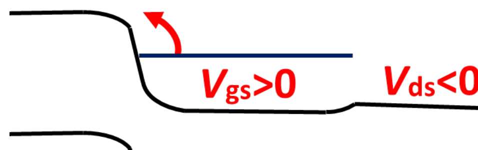


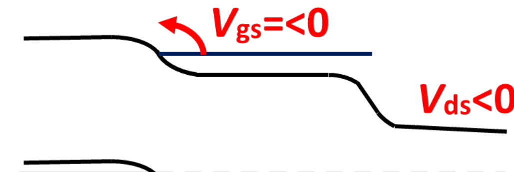


(2) S-D forward bias conditions (V_{ds}<0)

(c) V_{gs}>0: *p-n* diode current is dominant.

(d) V_{gs}=<0: *p-n* diode current and I_g should be considered.

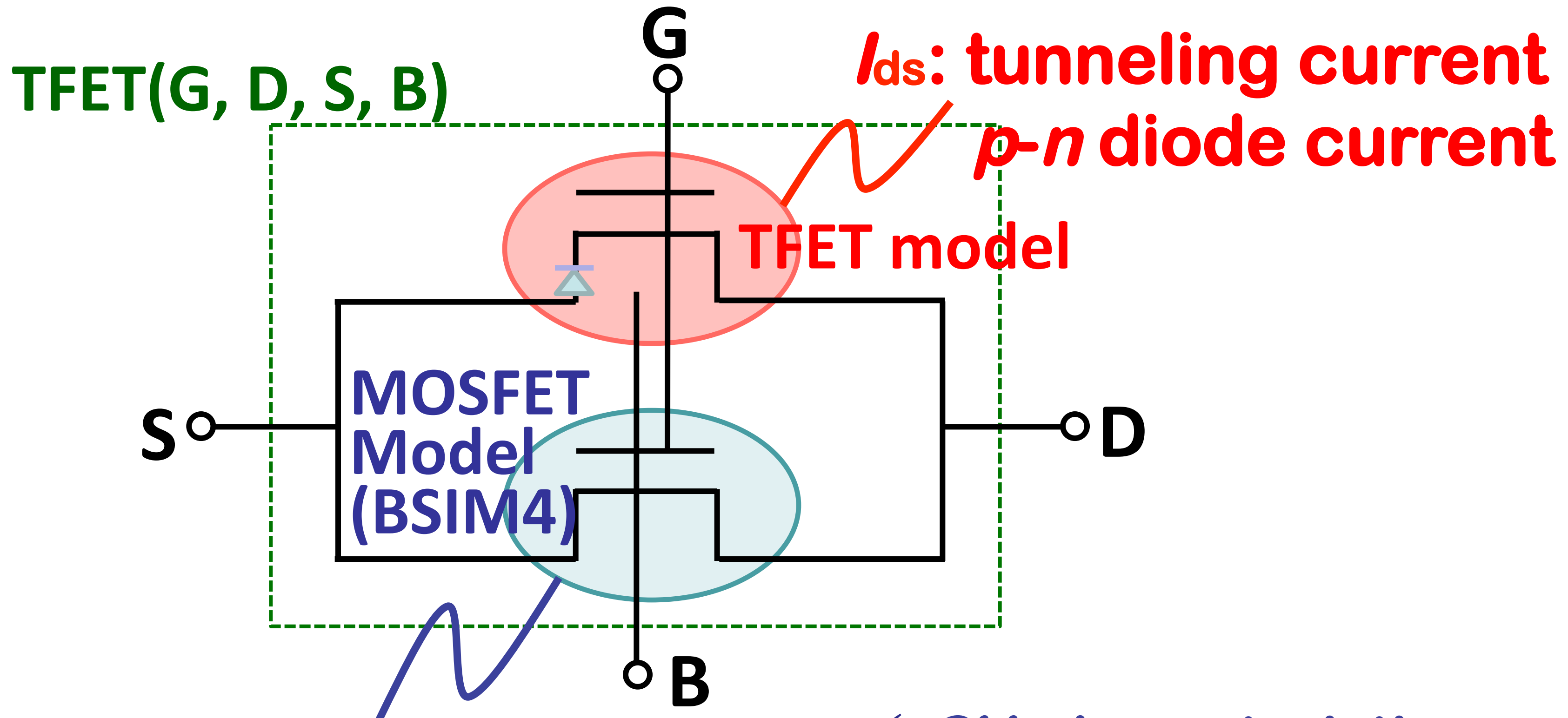




Our challenge:
Proposal of TFET compact model with simple device parameter which operates every bias conditions

Our concept: "TFET" model is combined with "MOSFET" (BSIM) model

To simulate the circuit operation of TFET,



I_{ds}: tunneling current
p-n diode current

I_g: gate leakage current,
I_j: junction leakage current

✓ *CV* characteristic:
Calibrated BSIM4 model parameters

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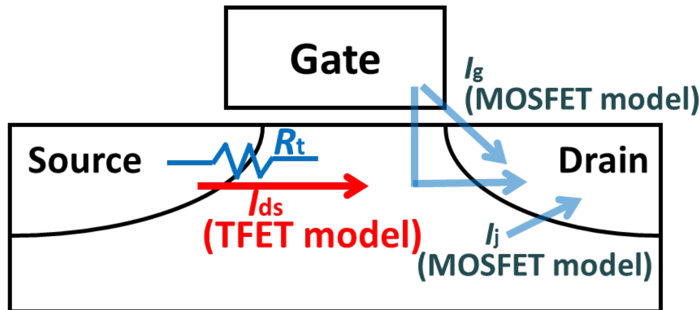
Tunneling current model



(1) If R_t is efficiently large, $Q_{channel} \sim Q_{tunnel}$.

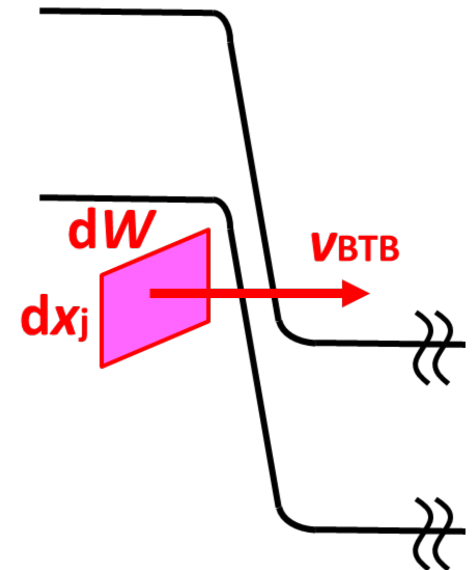
(2) based on a drift-diffusion model under the gradual-channel approximation

BTB tunneling current

$$J_{BTB} = \frac{\sqrt{2m^*}\, q^3}{4\pi^3 \hbar^2 \sqrt{E_g}} \cdot \exp\left(-\frac{4\sqrt{2m^*}\, E_g^{3/2}}{3q\hbar E_t}\right) \cdot E_t \cdot V_{app},$$

$$E_t = \sqrt{2qN_a (V_g + \psi_{bi})/\varepsilon_{si}}$$

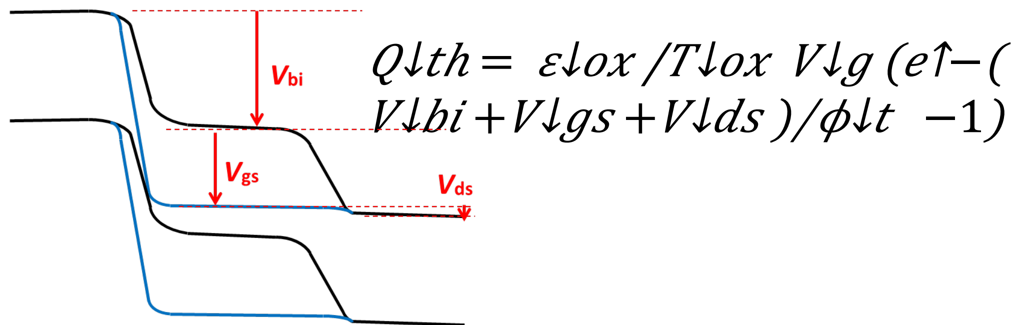
$$I_{BTB}/W = J_{BTB} \cdot x_j = Q_{tun} \cdot v_{BTB}$$



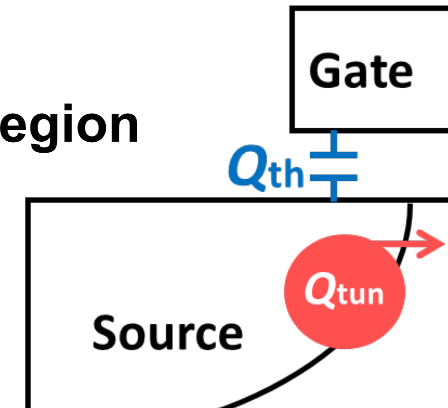
Total charge for the drain current (Q_0)

$$Q_0 = Q_{tun} f_1 + Q_{th} (1 - f_1)$$

Q_{th}: the oxide charge for gate-to-source overlap region



$$Q_{th} = \frac{\varepsilon_{ox}}{T_{ox}} V_g \left(e^{-(V_{bi} + V_{gs} + V_{ds})/\phi_t} - 1 \right)$$



f_1: smoothing function

(e.g. $1/(1 + e^{-x})$, where x represents the ratio L_g: L_{ov})

The total drain current (I_D) is represented using Q_0,

$$I_D / W = Q_0 \cdot v_{inj} \cdot F_s$$

“TFET model”: parameter list

Symbol		Unit
ϕ_{bi}	Built-in potential	V
E_g	Band gap	eV
T	Temperature	K
L	Channel length	m
W	Channel width	m
Xj	Junction depth	m
N	Substrate concentration of the tunnel junction	cm^{-3}

The advantage of our TFET model:

- **simple device parameter ->add various devise structure**
- **Representation of steep-*S* slope**
- **It will be available for every bias conditions.**

Our proposed model was implemented in SmartSpice using Verilog-A description.

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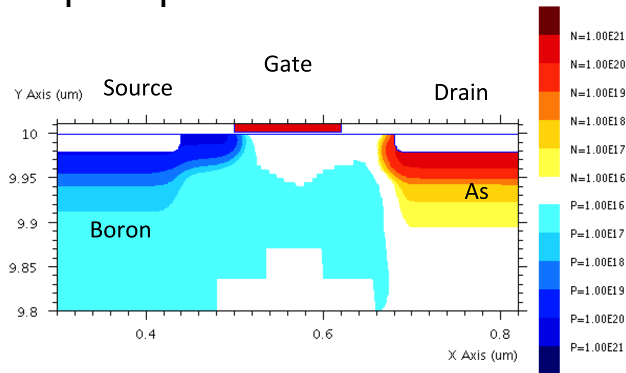
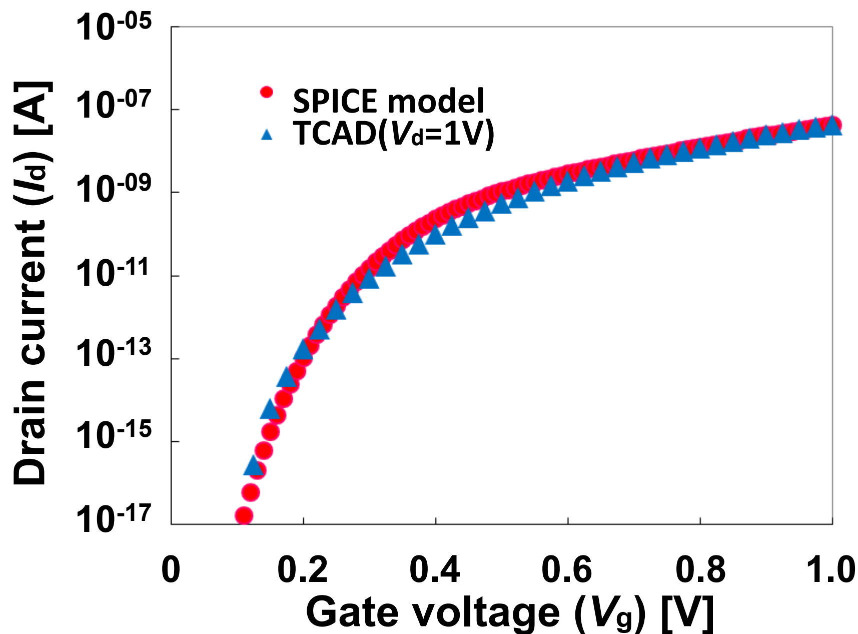
Simulation results: $I_d V_g$

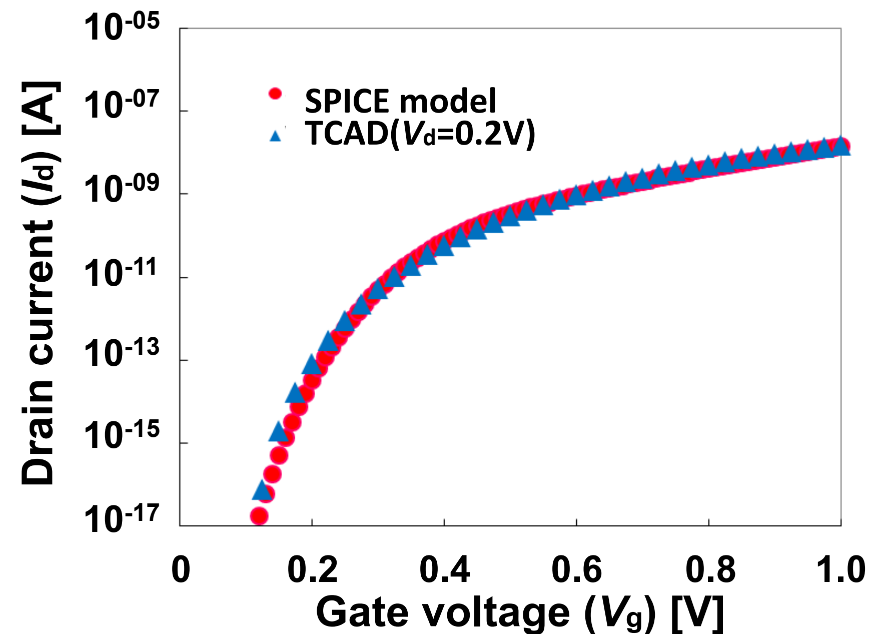
2D dopant profile for TCAD simulation



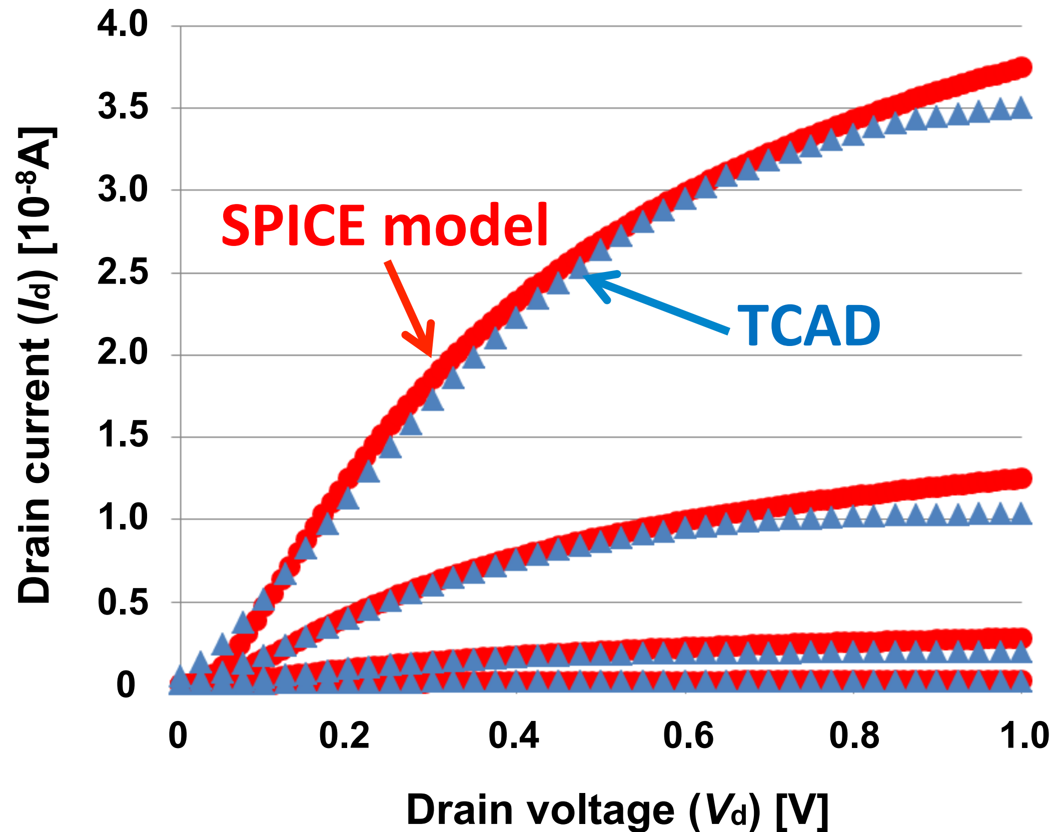
<u>TCAD simulation (in-house)</u>

- The device structure was formed to demonstrate the steep *S.S.* of 50mV/ decade.
- The ideal I_{on} required for the low-power operation.
- L_g=120nm, T_{ox}=2nm, N_s=1e16 cm^{-3}



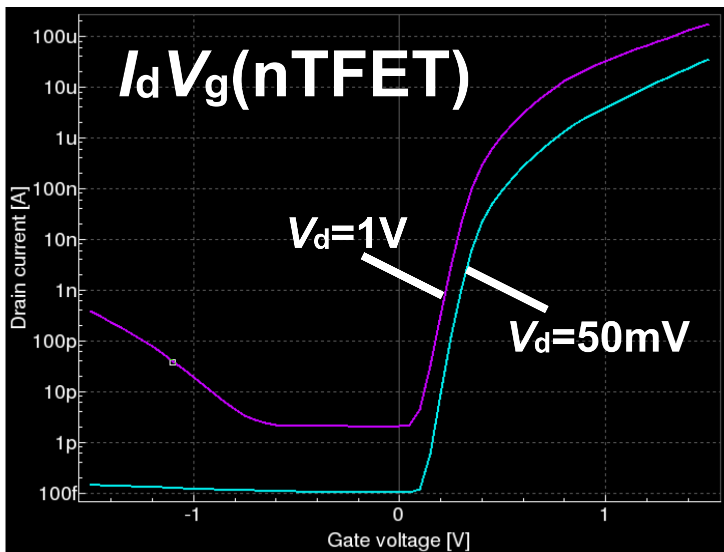


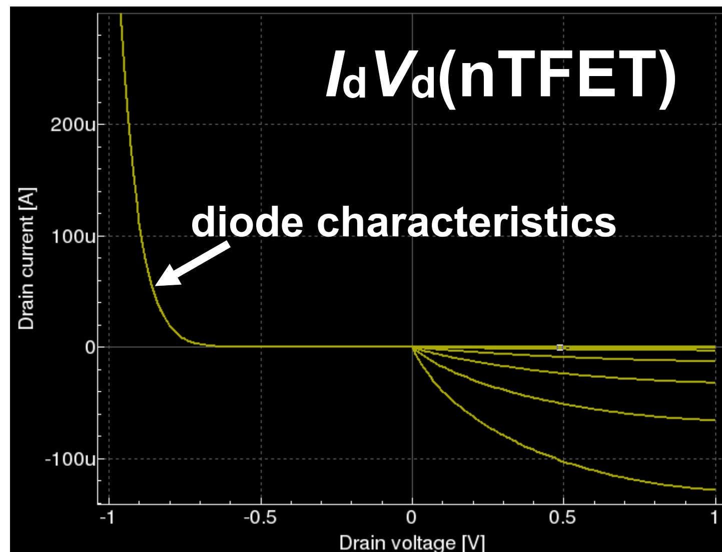
Simulation results: $I_d V_d$

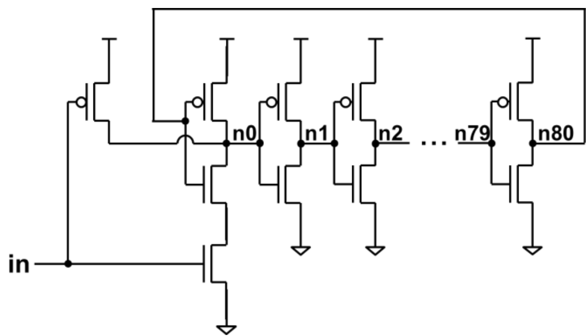


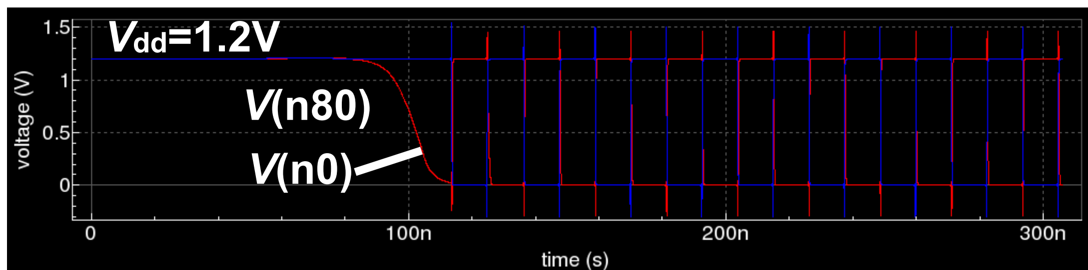
Our model shows a good agreement with TCAD in the targeted operating voltage range.

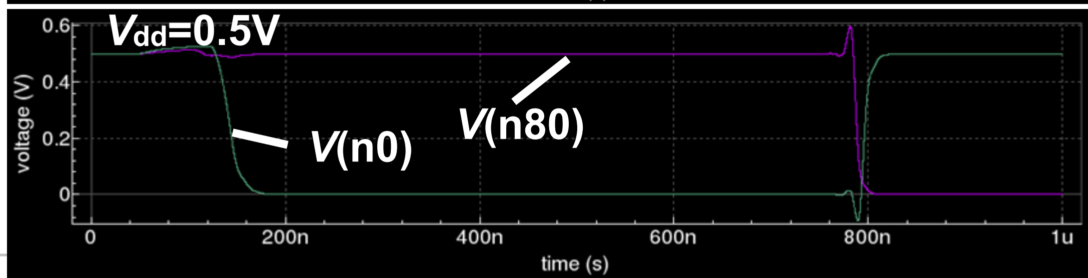
Circuit simulation results











Summary

- **Compact model of tunneling field effect transistor was proposed.**
  - Our *"TFET model"* combined with *"MOSFET BIMS4 model" by parallel connection.*
  - It was available for *every bias conditions.*
  - implemented in circuit simulator *using Verilog-A description.*

our proposed model is useful tool for the circuit-level analysis.

Acknowledgement
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