



Full Development Chain of Compact Modeling

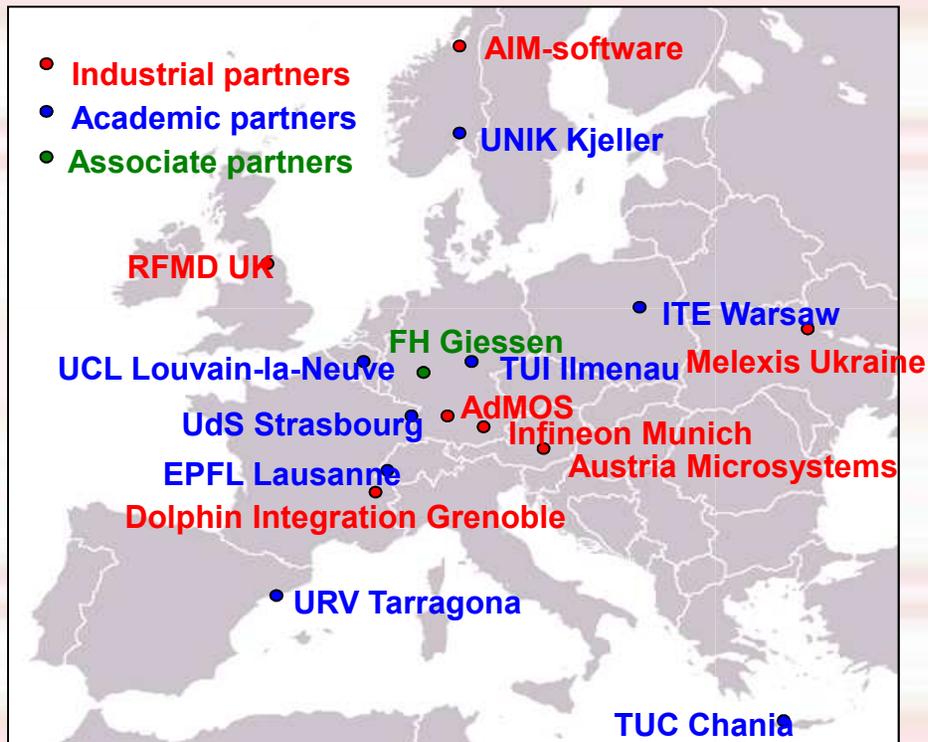
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UNIVERSITAT
ROVIRA I VIRGILI

EU COMON Project – Who are we?

COMON: COmpact MOdeling Network



✓ “Marie-Curie”
Industry-Academia
Partnership and
Pathways project (IAPP
FP7, ref. pro. 218255)

✓ Duration:
4 years, started from
Dec 1 2008.

✓ Coordinator:
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➤ More information available on our website:
<http://www.compactmodelling.eu>

Goals



To address the **full development chain** of Compact Modeling, to develop complete compact models of **Multi-Gate MOSFETs** (Foundry: Infineon), **HV MOSFETs** (Foundry: Austriamicrosystems) and **III-V FETs** (RFMD (UK)).

Development of **complete compact models (CM)** of these types of advanced semiconductor devices.

Development of **suitable parameter extraction** techniques for the new compact models.

Implementation of the compact models and parameter extraction algorithms in automatic circuit design tools.

Demonstration of the implemented compact models by means of their utilization in the design of test circuits.

Validation and benchmarking: compact model evaluation for analog, digital and RF circuit design: convergence, CPU time, statistic circuit simulation.

As an IAPP project the ultimate COMON goal is the know-how transfer from the academia to the industry

COMON as a Network



- ◆ COMON is a communication platform for foundries, software vendors, circuit designers and universities regarding CM issues.
- ◆ COMON has established a joint programme to enable research through intersectorial and multidisciplinary collaboration, including researcher exchanges between academia and industry, as well as training activities.
- ◆ COMON industrial partners will be able to take advantage of the new CM during the course of the project and start applying the new tools for production shortly after the end of the project.
- ◆ The incorporation of the new CM in the PDKs of modern semiconductor foundry partners will lead to faster and cost effective IC development cycles and higher integration levels.

Working Groups



- ◆ The COMON Network consist of three Working Groups (WGs). Each WG addresses one specific targeted Compact Model (CM) of the semiconductor device. WG is composed of the partners who work on the different Work Packages related to that specific device

- ◆ **WG1: Multiple-Gate SOI MOSFETs**
 - ◆ UCL, URV, UniK, EPFL, UdS, TUC, ITE, Infineon (now Intel), AdMOS, AIM-Software
- ◆ **WG2: High Voltage MOSFETs**
 - ◆ AMS, EPFL, TUC, AdMOS, Dolphin, Melexis, AIM-Software
- ◆ **WG3: Advanced III-V HEMTs**
 - ◆ TU-Ilmenau, UniK, URV, RFMD , AIM-Software

- ◆ Annual meetings for every WG are held to discuss and coordinate the work for each specific device

Activities funded by COMON

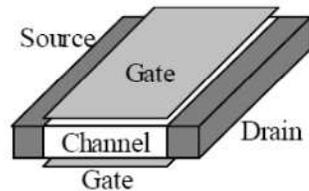


- Secondments of young researchers between academia and industry
 - Universities sending students to the participating companies for several months
 - Also, several companies sending employees to universities for trainings
 - Secondments are the most instrumental tool for the transfer of knowledge between academia and industry
- Recruitments of postdoctoral researchers from outside the COMON network
- MOS-AK Workshops in Europe
- Training Courses on Compact Modeling
 - 1st Course, held in Tarragona (Spain) on June 30-July 1 2010
 - **2nd Course, to be held Tarragona (Spain) on June 28-29 2012**

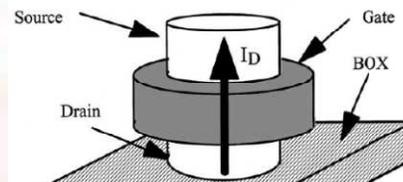
Multi-Gate MOSFETs



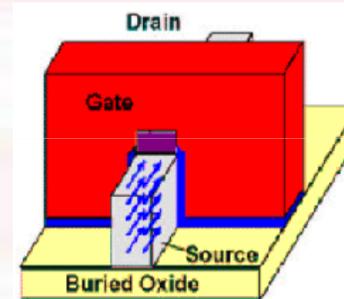
- The non-classical multi-gate devices such as Double-Gate (DG) MOSFETs, FinFETs or Gate-All-Around (GAA) MOSFETs show an even stronger control of short channel effects, and increase of on-currents taking advantage of volume inversion/accumulation.



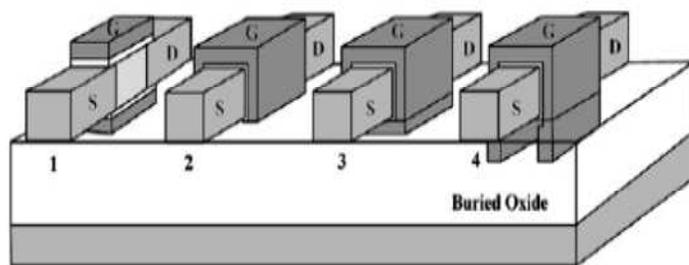
DG MOSFET



GAA MOSFET



FinFET



Schematic device structures of MuGFETs: 1) double-gate; 2) triple-gate; 3) quadruple-gate; 4) PI-gate

Modeling Approaches



- 1) A purely design-oriented model developed by UCL/URV for symmetric DGMOSFETs. It is based on a 1D electrostatic analysis with semi-empirical equations with fitting parameters for short-channel effects. It can work for FinFETs and Tri-Gate MOSFETs if they are narrow enough.
- 2) A “mixed” predictive design-oriented model developed by UdS/EPFL with the recent collaboration from URV. It was originally a quasi-2D model for DG MOSFET that now is becoming a quasi-3D model for Tri-Gate MOS structures. It uses very few fitting parameters and is explicit.
- 3) A fully 2D/3D predictive model, based on isomorphic expressions, developed by UniK in cooperation with URV. It is a predictive technology-oriented semi-analytical model.

Core (1D) undoped DG MOSFET Model



- An analytical solution is possible in the case of undoped DG MOSFET or cylindrical Surrounding-Gate MOSFETs
- For undoped DG MOSFETs, Poisson's equation:

$$\frac{d^2\psi(x)}{dx^2} = \frac{d^2(\psi(x) - V)}{dx^2} = \frac{q}{\epsilon_{Si}} \cdot n_i \cdot e^{\frac{q(\psi(x) - V)}{kT}}$$

- The resulting charge control model can be written as:

$$(V_{GS} - V_0 - V) = \frac{Q}{C_{ox}} + \frac{kT}{q} \log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q} \log\left(\frac{Q + Q_0}{Q_0}\right)$$

Design-Oriented Model for Multi-Gate MOSFETs

Model developed as a collaboration between UCL (Belgium), URV (Spain) and CINVESTAV (Mexico).

Model dedicated to the simulation of analog and mixed signal circuits using DG MOSFETs, than can also be applied to FinFET as well as trigates structures with a narrow width fin.

The model equations are based on **analytical expressions of the potentials**, that allow continuity in all operation regions for undoped and doped silicon layers.

Several effects are taken into account in the model, like geometrical and process related aspects (oxide thickness, width fin, high fin, polysilicon and midgap metal gates), effects of doping profile, mobility effects due to the vertical and longitudinal fields, short-channel effects due to velocity saturation, channel-length modulation, roll-off and DIBL and temperature effects.

Design-Oriented Model for Multi-Gate MOSFETs

The model is continuous from weak to strong inversion, as well as from linear to saturation regimes, and it incorporates the internal capacitances, as well as fringing capacitances.

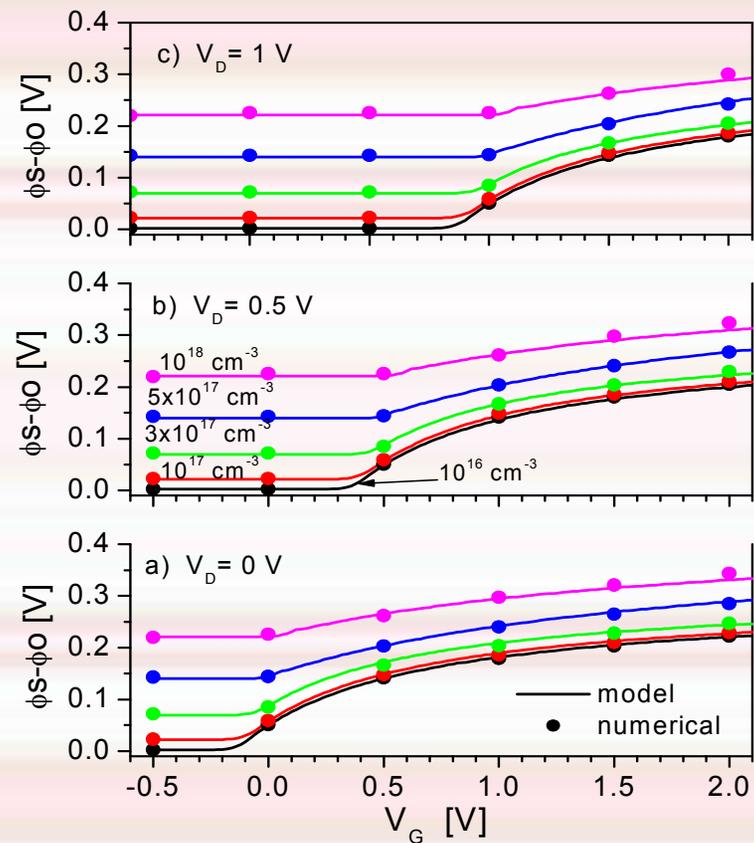
The model is based on a charge control model for long-channel DG MOSFET from which drain current and charge models are developed. Charge sheet densities at source and drain are calculated from explicit potential expressions

Semi-empirical continuous expressions are used to account for short-channel effects: subthreshold swing degradation, threshold voltage roll-off, DIBL

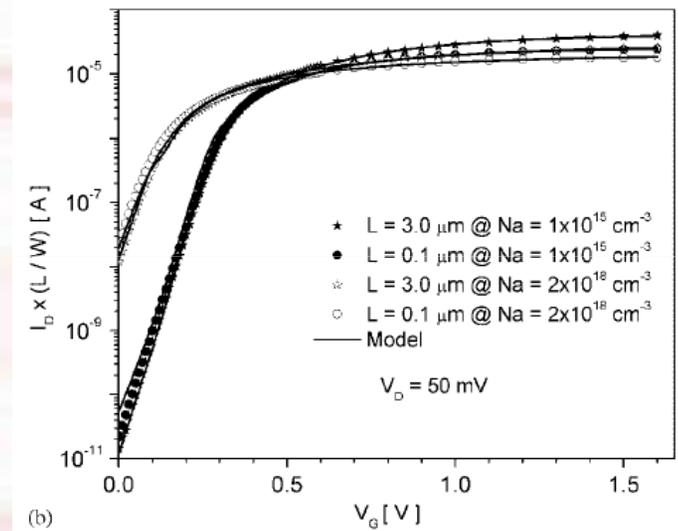
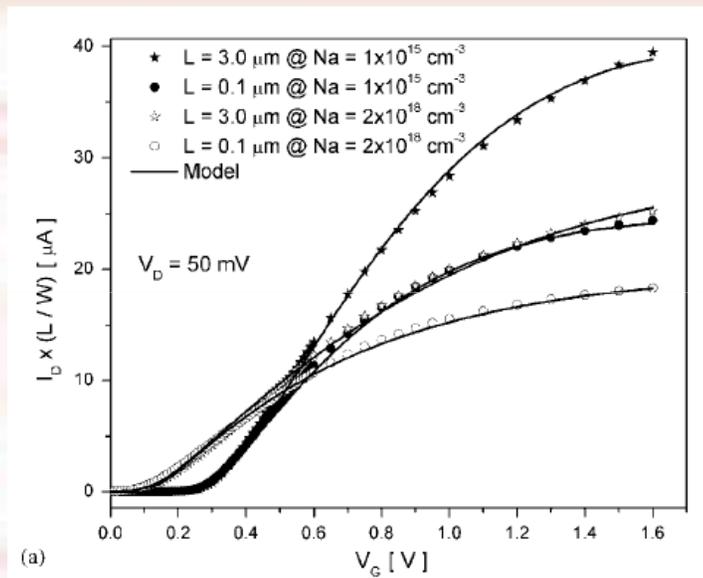
Its main features are:

- a) A good agreement in all operation regions for I-V and C-V curves is ensured for channel lengths in the range of ($50\text{nm} < L$),
- b) The maximum value allowed for doped devices is $N_A = 2 \cdot 10^{18} \text{ cm}^{-3}$;

Core DG MOSFET model - Calculation of $\phi_d = \phi_s - \phi_o$ in all regions

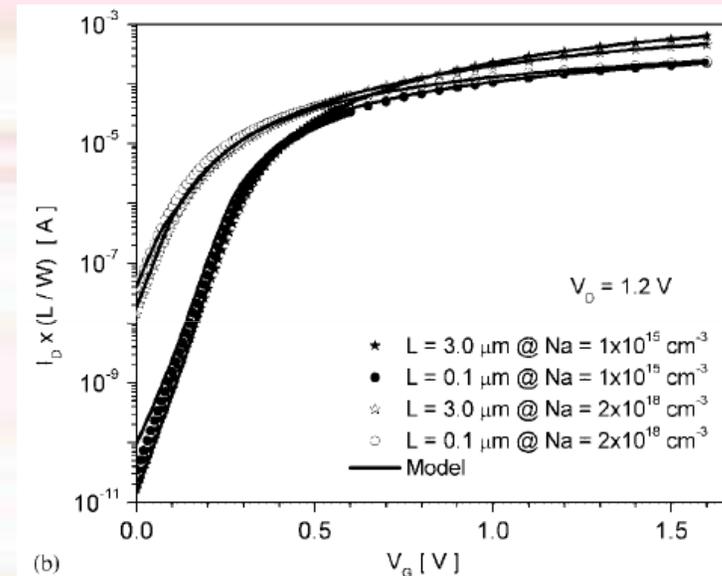
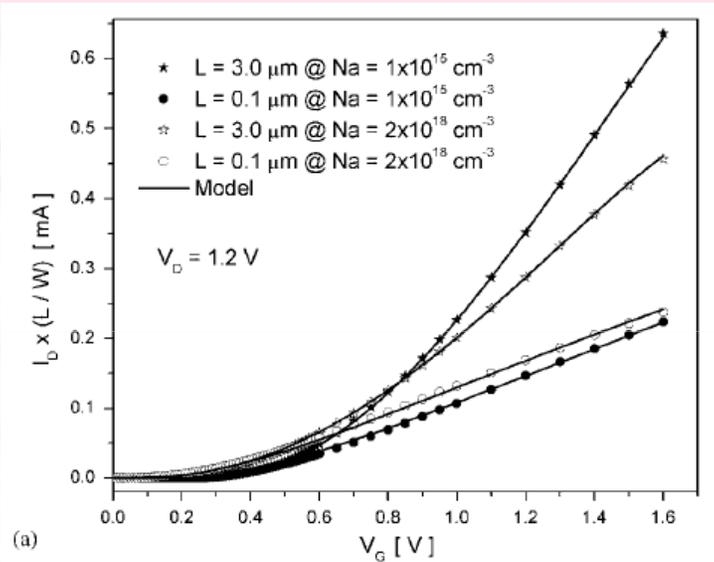


Design oriented DG MOSFET model



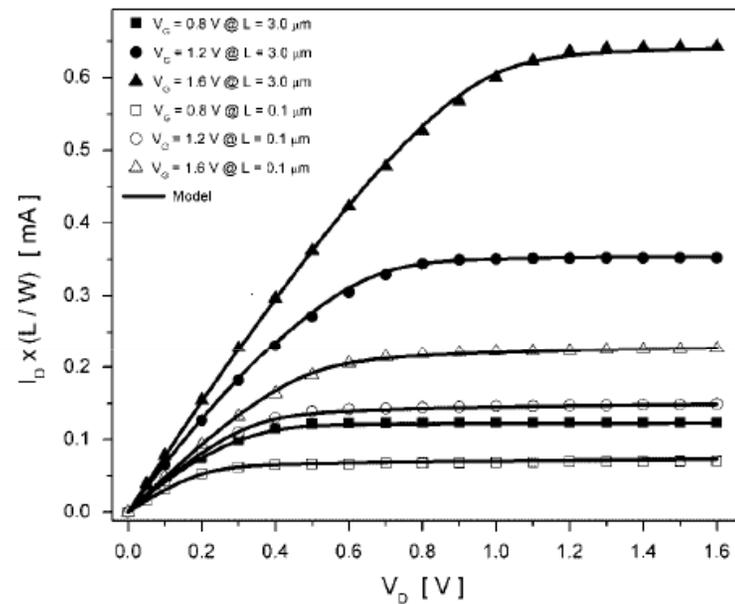
Simulated and modeled transfer characteristics for 3 μm and 100nm channel lengths at $V_D=50$ mV: (a) I-V curves and (b) semilog I-V curves.

Design oriented DG MOSFET model

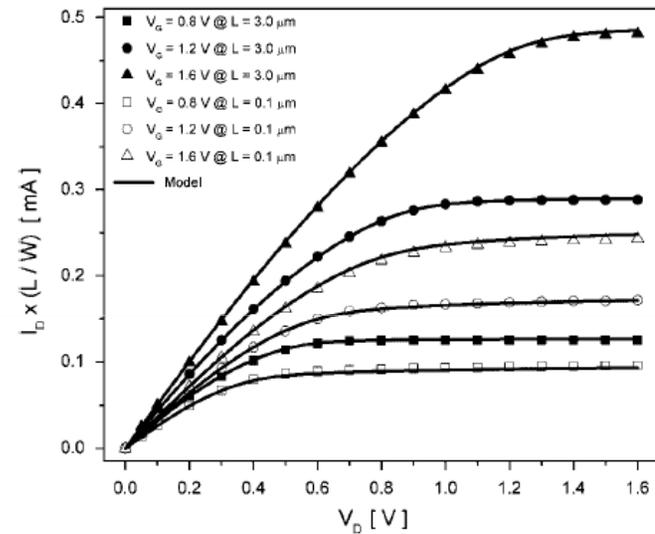


Simulated and modeled transfer characteristics for 3 μm and 100nm channel lengths at $V_D=1.2$ V: (a) I-V curves and (b) semilog I-V curves.

Design oriented DG MOSFET model



Simulated and modeled normalized output characteristics of 3 μm and 100nm channel lengths at $V_G = 0.8, 1.2$ and 1.6 V for $N_a = 1 \times 10^{15} / \text{cm}^3$.



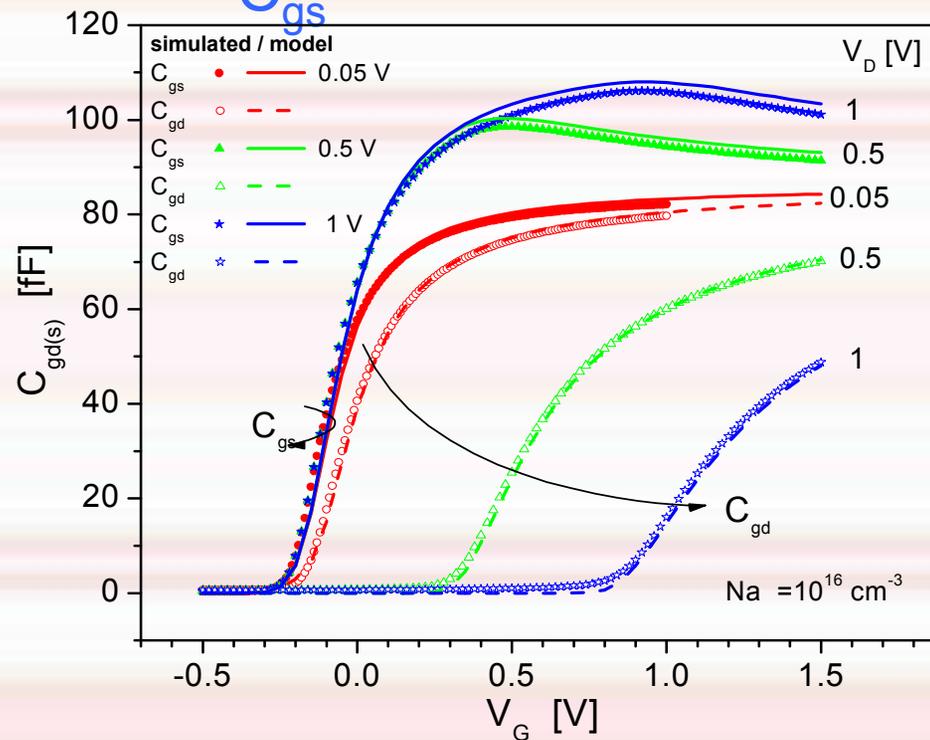
Simulated and modeled normalized output characteristics of 3 μm and 100nm channel lengths at $V_G = 0.8, 1.2$ and 1.6 V for $N_a = 2 \times 10^{18} / \text{cm}^3$.

Capacitance model

$L = 5 \mu\text{m}$

$\mu = 400 \text{ cm}^2/\text{Vs}$

Modeling of C_{gd} and C_{gs}



Mixed Predictive Design Oriented Multi-Gate MOSFET Model



The UdS and EPFL teams developed a strongly physically-based and explicit compact model for lightly doped FinFETs, which has been extended to doped devices.

It is a design-oriented model valid for a large range of silicon Fin widths and lengths, using only a very few number of model parameters.

The model is based on a core charge control model derived from the 1D Poisson's equation, with extensions coming from the remaining 2D/3D Poisson's equation.

The quantum mechanical effects (QMEs), which are very significant for thin Fins below 15 nm, are included in the model as a correction to the surface potential.

Mixed Predictive Design Oriented Multi-Gate MOSFET Model

A physics-based 2D/3D approach is followed to model short-channel effects (roll-off), drain-induced barrier lowering (DIBL), subthreshold slope degradation, using hyperbolic functions.

Velocity saturation, channel length modulation and carrier mobility degradation are also included.

The quasi-static model is then developed and accurately accounts for small-geometry effects as well.

Mixed Design Oriented Multi-Gate MOSFET Model: Short-Channel Effects



Validity of the extended model:

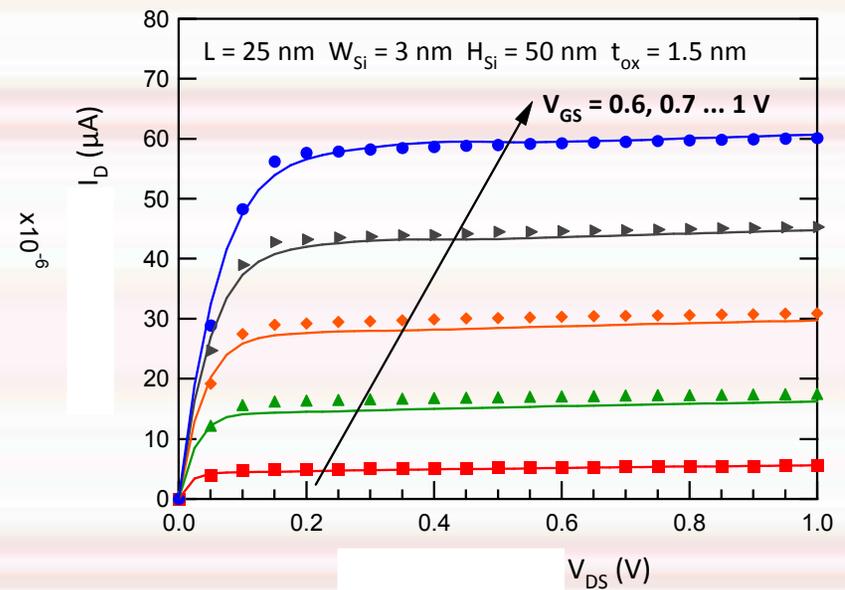
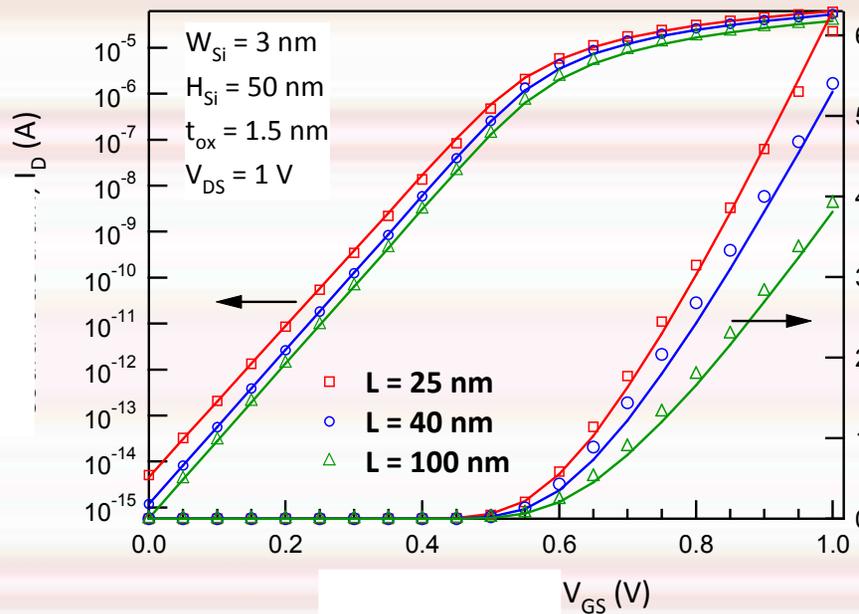
Gate length (L): down to 25 nm

Silicon width (W_{Si}): down to 3 nm

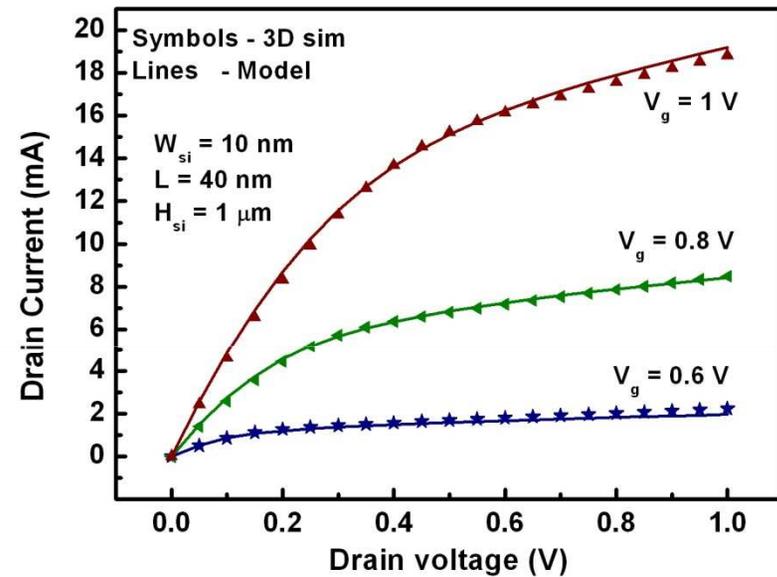
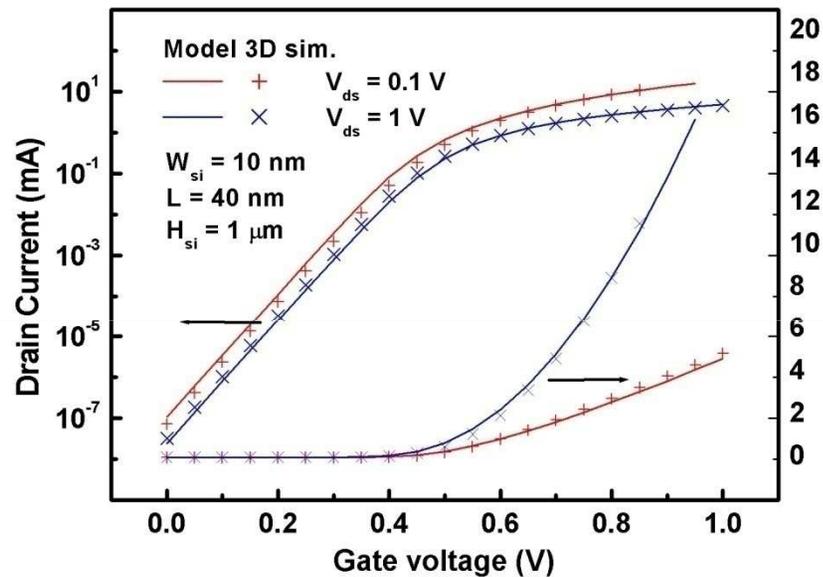
Silicon height (H_{Si}): down to 50 nm

Channel doping (N_a): intrinsic to 10^{17} cm^{-3}
nMOS and pMOS

Mixed Predictive Design Oriented Multi-Gate MOSFET Model



Mixed Predictive Design Oriented Multi-Gate MOSFET Model:

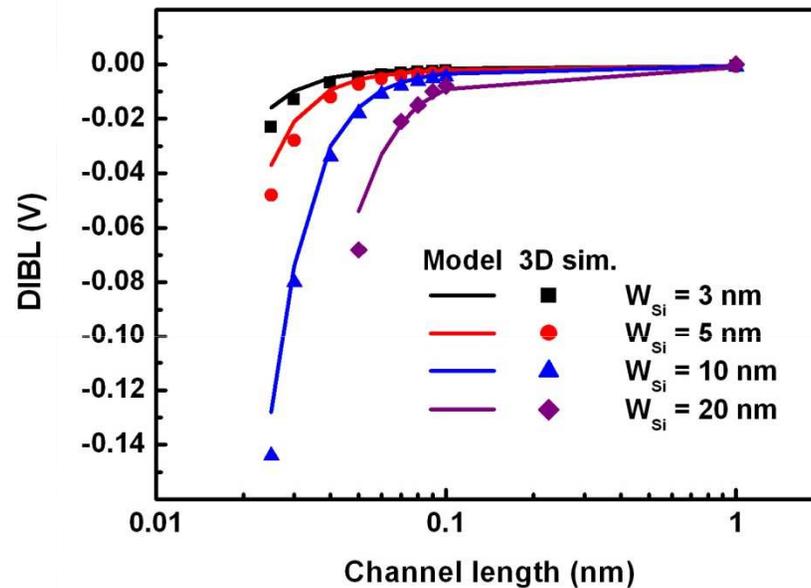
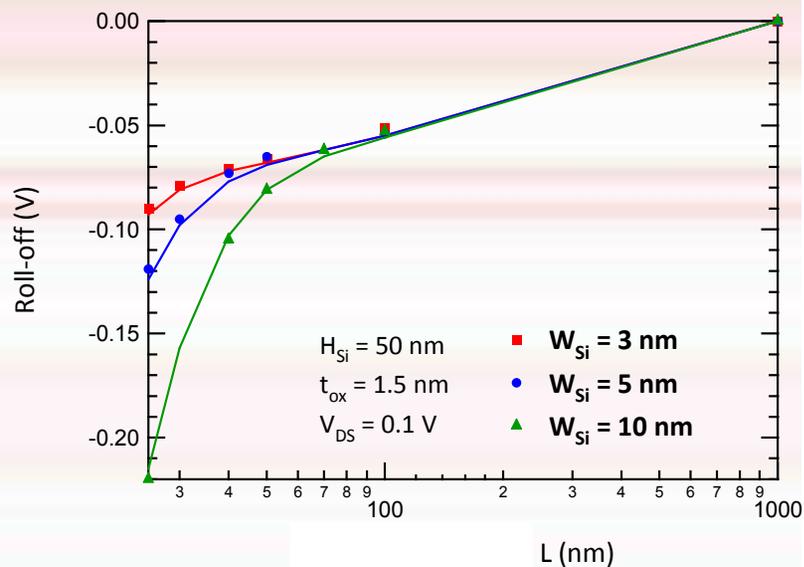


Lines: compact model; symbols: TCAD simulations.

The above figures are w/o QME and with a constant mobility.



Mixed Predictive Design Oriented Multi-Gate MOSFET Model



Influence of the channel width W_{Si} on both roll-off and DIBL. A thinner silicon film is desirable to limit short-channel effects. However, let us note that quantum effects play a major role for $W_{Si} < 10$ nm.

QME are not accounted for in the above figures in order to focus only on SCE.



2D/3D Predictive Multi-Gate MOSFET Modeling

Objectives:

- Establish unified analytical models for nanoscale MugFETs (multigate MOSFETs) including FinFET and GAA devices The model was developed by UniK and URV

Procedure :

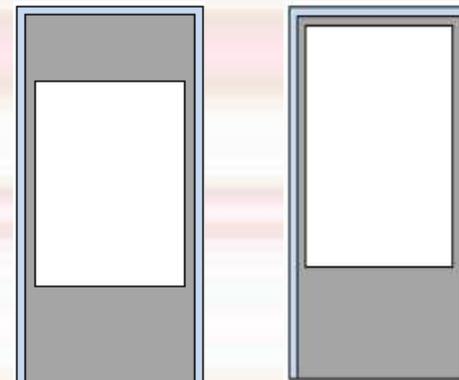
- Decompose Poisson's equation into a Laplace equation and a residual Poisson's equation (superposition principle)

Capacitive inter-electrode effects

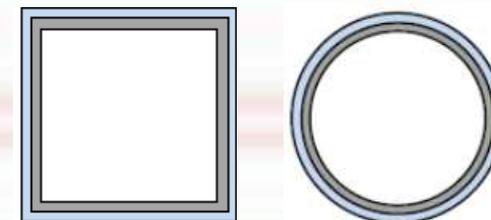
- From 2D/3D Laplace equation determine potential distribution associated with capacitive inter-electrode coupling.
- Use this to calculate *subthreshold* electrostatics, drain current and capacitances

Near and above threshold

- Apply residual Poisson's equation, boundary conditions, and modeling expressions to determine *self-consistent* device properties



Schematic representation of 2D cut-plane of DG FinFET and trigate FinFET respectively



Schematic representation of 2D cut-plane of quad- and cylindrical GAA devices respectively



2D/3D Predictive Multi-Gate MOSFET Modeling

The final model is based on the use of *isomorphic modeling* expressions for the potential distribution in (x,y) cross sections perpendicular to the source-drain z axis.

In subthreshold, this allows the complete potential distribution in the device body to be obtained based on the Laplace equation.

Short-channel effects are included by introducing auxiliary boundary conditions, such as the device center potential and the electrical field at the source center, derived analytically from the conformal mapping analysis



2D/3D Predictive Multi-Gate MOSFET Modeling

A similar procedure, again using isomorphic modeling expressions, can also be applied to strong inversion by invoking Poisson's equation.

Starting from a rectangular gate structure, the present modeling can be generalized to include FinFETs, trigate, square gate, DG, and even circular gate devices, laying the groundwork for a unified, compact modeling framework for a wide range of multigate MOSFETs.



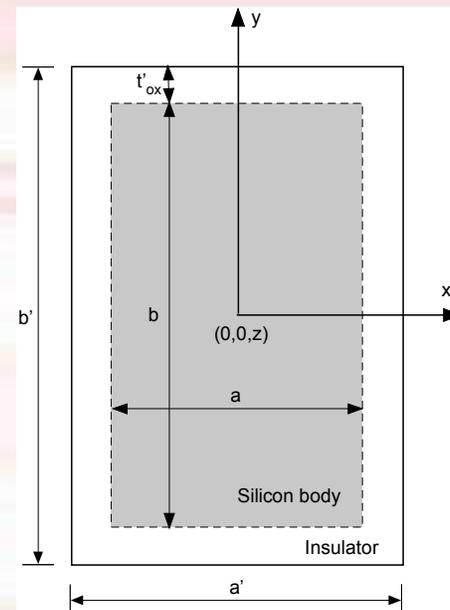
2D/3D Predictive Multi-Gate MOSFET Modeling

We first consider a MugFET with a rectangular (x,y) cross-section of silicon widths a and b , for which we write the potential distribution as a 'power expansion' of the following isomorphic form,

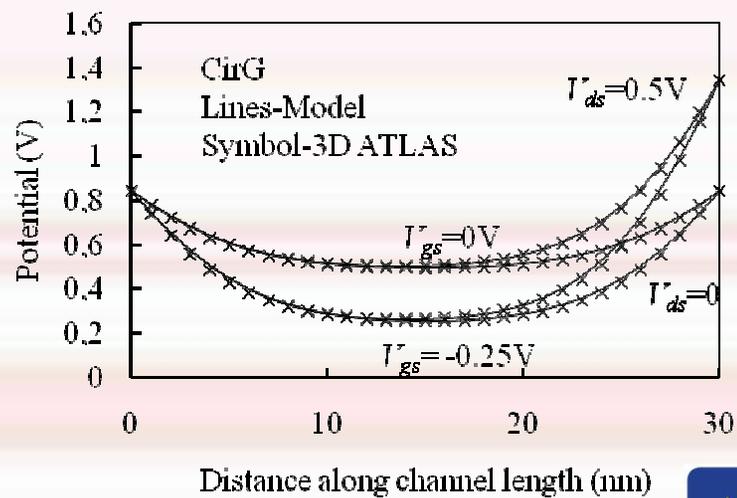
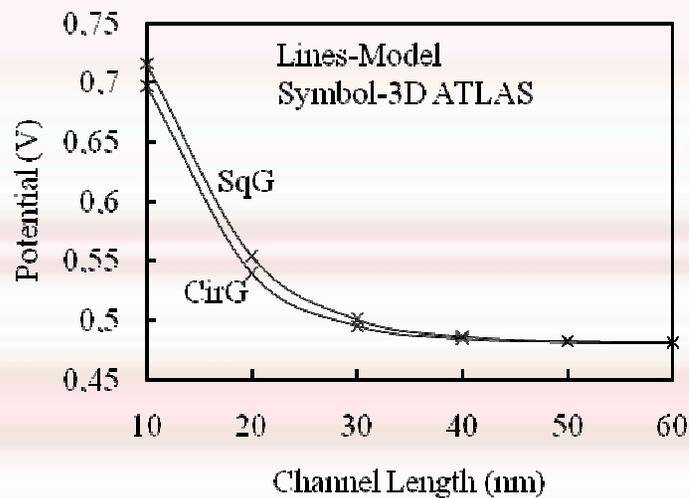
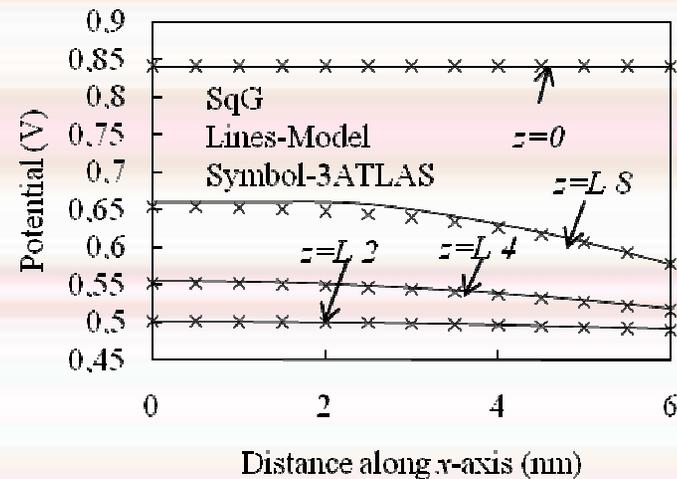
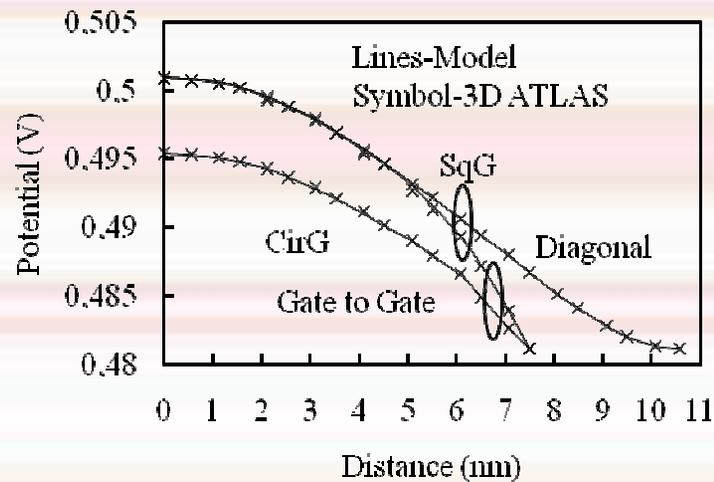
$$\hat{\phi}(x, y, z) = \hat{\phi}(0, 0, z) \sum_{i=1}^n \alpha_i \left[1 - \left(\frac{2x}{a'} \right)^{2i} \right] \left[1 - \left(\frac{2y}{b'} \right)^{2i} \right]$$

Here $a' = a + 2t'_{ox}$, $b' = b + 2t'_{ox}$ and $t'_{ox} = t_{ox} \epsilon_{si} / \epsilon_{ox}$ is an equivalent silicon layer that represents the electrostatic effect of the true gate insulator

$\hat{\phi}(x, y, z)$ is the body potential relative to the gate interface.



3D GAA MOSFETs (modeling results)



FinFET Modeling

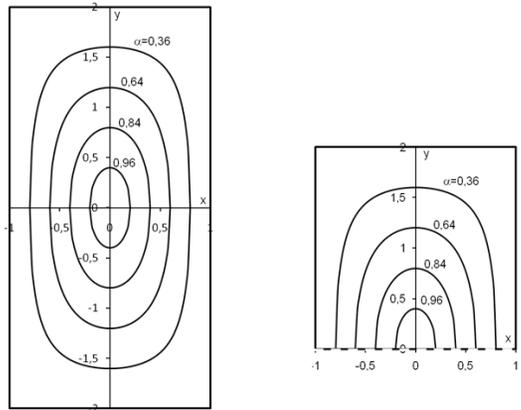


Trigate FinFET

The modeling of the trigate FinFET is based on the observation that this structure is a symmetric half of a rectangular GAA device.

Remedy to correct electrostatics

- Use results from RecG device (rectangular GAA) to obtain ground plane potential distribution of trigate FinFET
- Model the center plane of trigate FinFET, which corresponds to $H_{rec}/4$ above the center plane of the rectangular GAA device with an adjusted scaling length λ

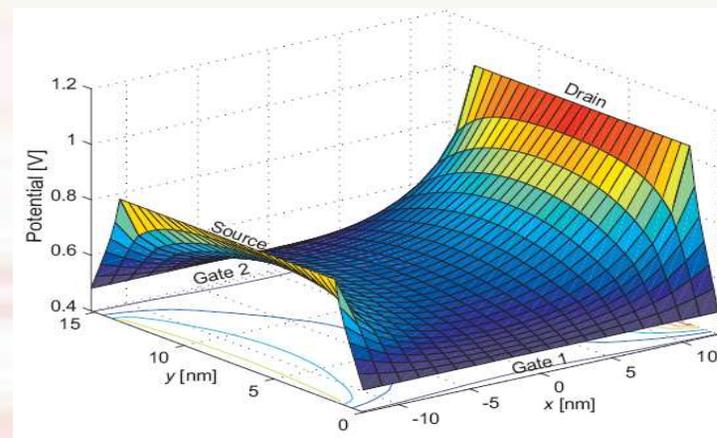


Equipotential contours in (x,y) cross sections of a rectangular GAA MOSFET and the corresponding trigate MOSFET

DG (double gate) FinFET

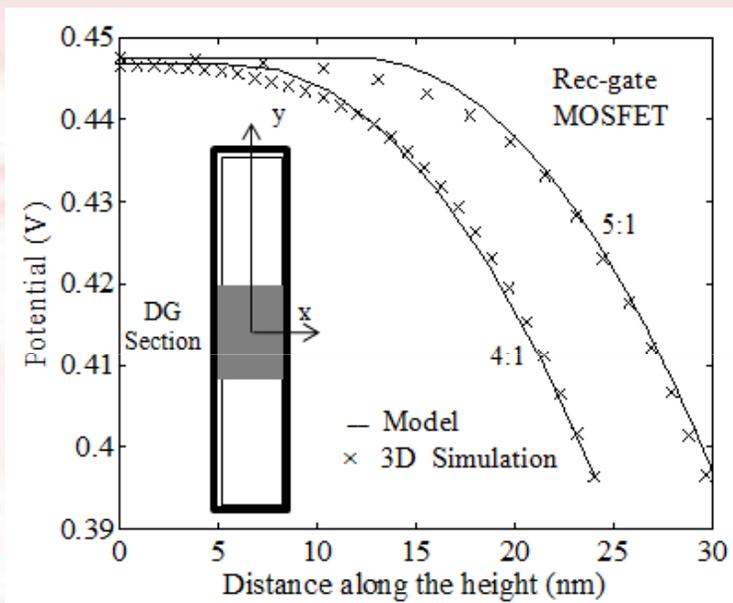
In case of DG FinFETs, the height to width ratio is quite large and the top electrode is separated from the channel by a thick oxide, hence the variation of potential along the fin height is negligible

2D solution can thus be directly extended to 3D device

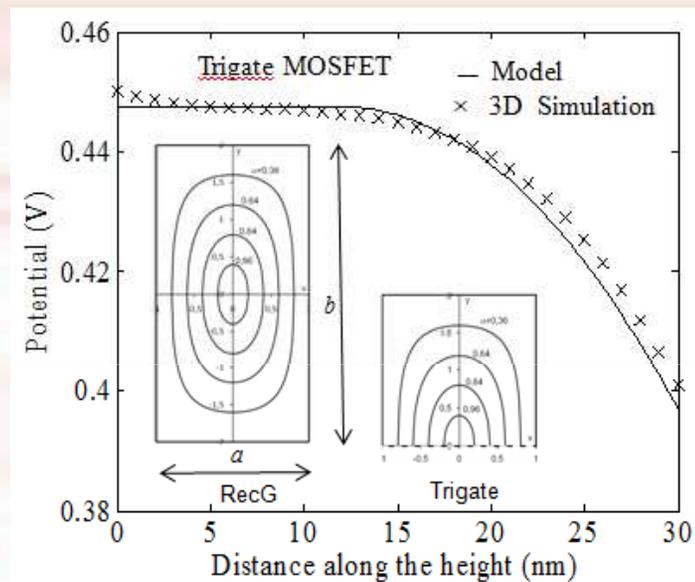


2D potential distribution in double-gate device at $V_{GS} = V_{DS} = 0.2 \text{ V}$

FinFET modeling

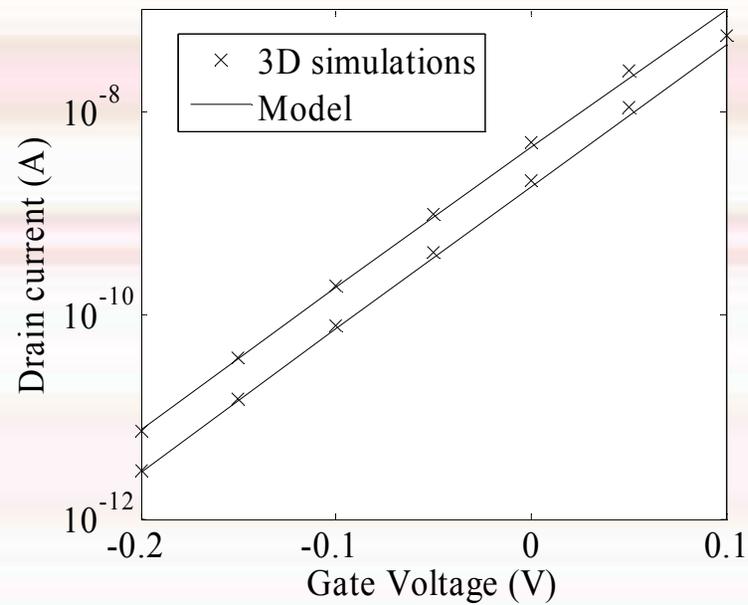


Modeled potential compared to numerical simulations along the height (y) direction for rec-gate devices with $\kappa = 4$ and 5 , $V_{ds} = 0$ V, $V_{gs} = -0.1$ V.



Modeled potential compared to numerical simulations along the height direction for a trigate device. Aspect ratio of original rec-gate device: 5:1. $V_{ds} = 0$ V, $V_{gs} = -0.1$ V

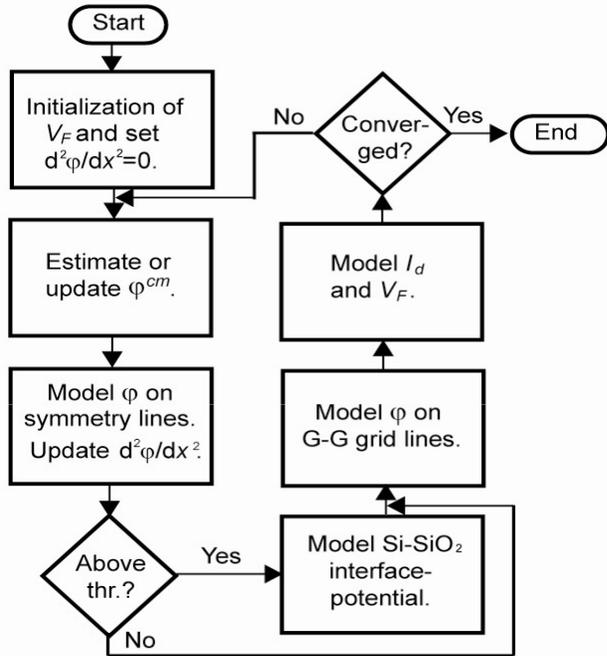
FinFET modeling



Modeled subthreshold current in trigate MOSFET, compared with the numerical simulations. Aspect ratio of original rec-gate device: 5:1.



Near-threshold and Strong Inversion Modeling



The iterations are computationally efficient!

In strong-inversion, the device attains long channel behavior, and can be modeled as a long-channel device

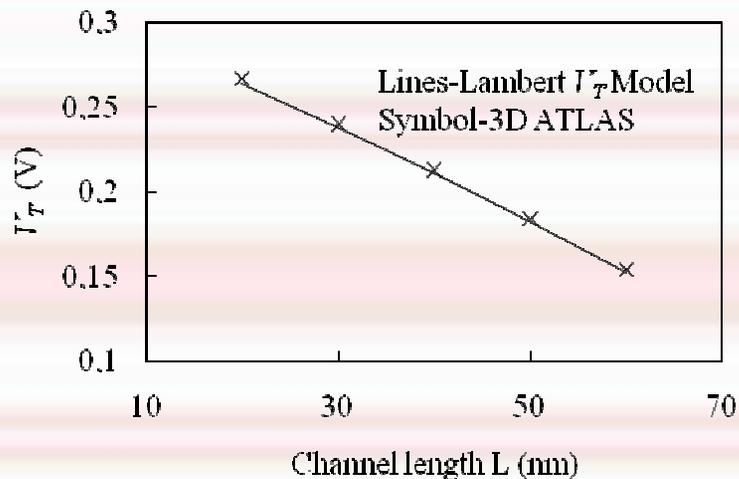
Transition (threshold) voltage ($V_{DS} = 0V$):

Defined as the gate voltage for which center G-G potential becomes flat– pseudo flatband condition

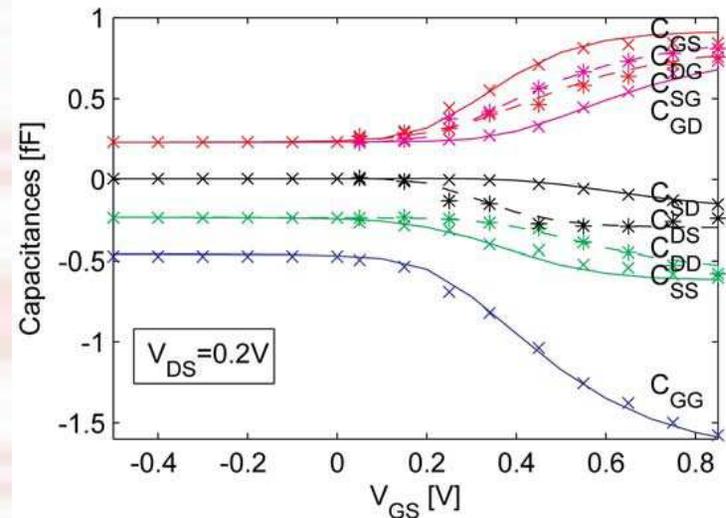
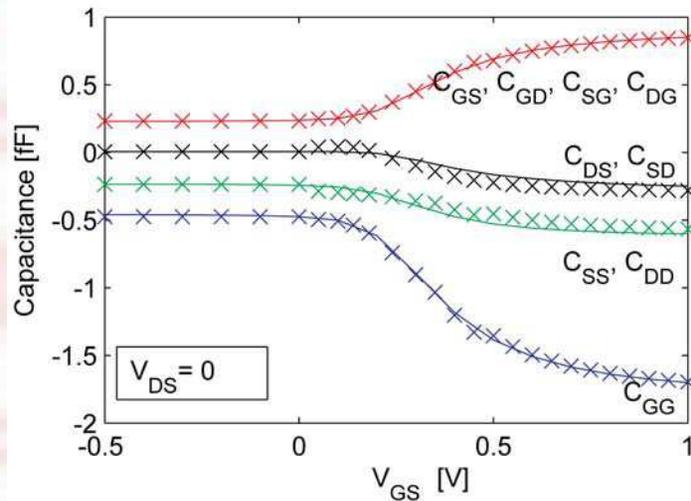
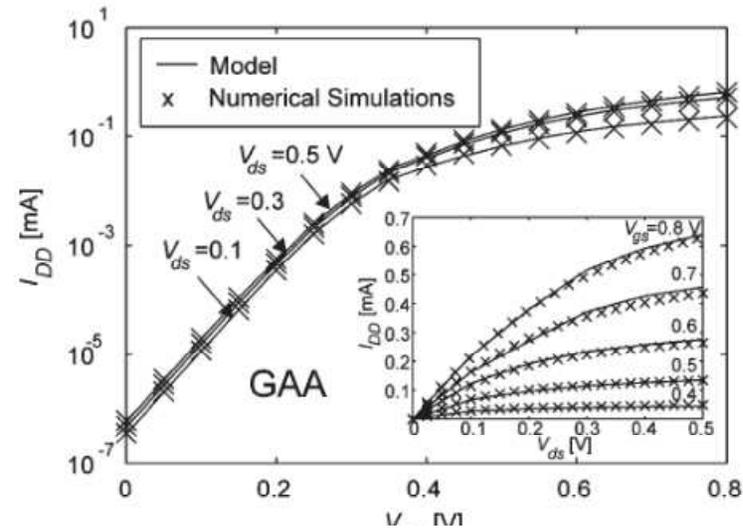
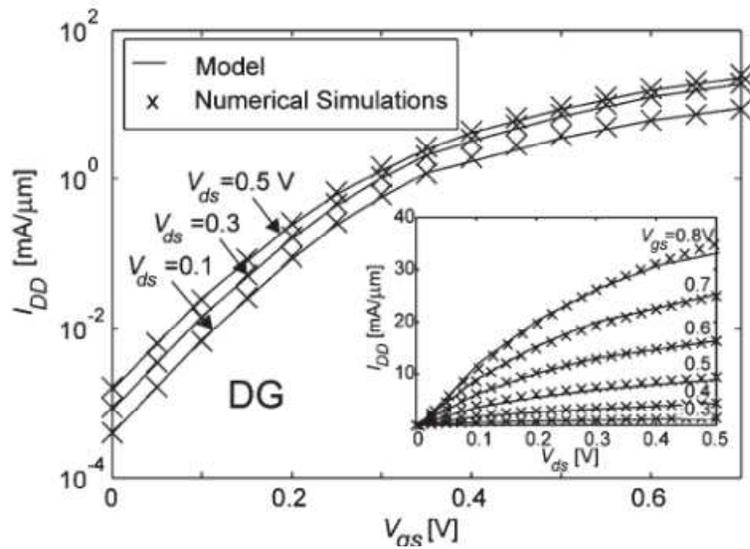
Unified equation for transition voltage:

$$\frac{V_{bi} - V_T + V_{FB}}{V_{th}} \exp\left(\frac{V_{bi} - V_T + V_{FB}}{V_{th}}\right) = \beta \left(\frac{V_{bi}}{V_{th}}\right)$$

β is a physical parameter dependent on device dimensions



Drain current and capacitance results



Other Multi-Gate MOSFET Modeling Issues

In addition, partners developed an analytical framework for several effects, that can be applied to any of the 3 models described before:

- 1) Self-heating
- 2) Low frequency noise
- 3) High frequency (thermal) noise
- 4) High frequency behavior
- 5) Gate and GIDL currents

High Voltage MOSFET Modeling

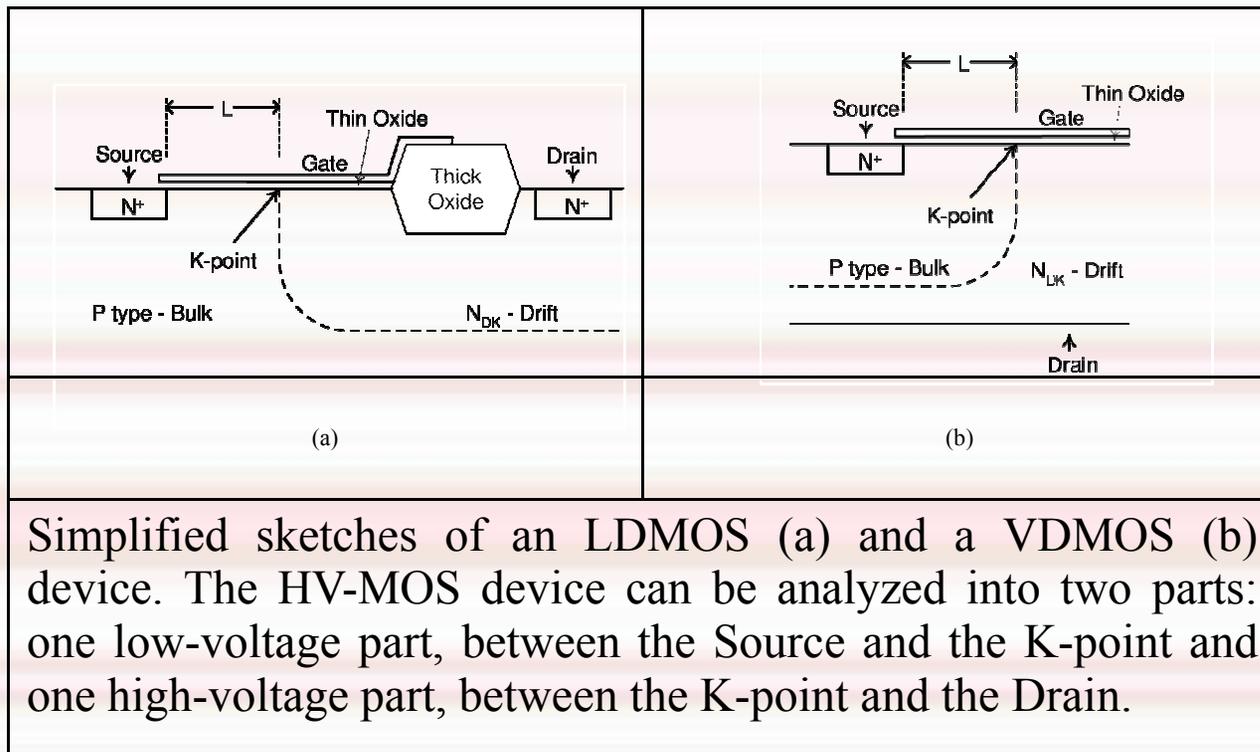
The HV-MOSFET model developed by COMON Working Group 2 (WG2) partners is a compact model built to describe the behavior of High Voltage MOSFETs.

It is made to cover both Lateral double-Diffused (LD) MOS and Vertical double-Diffused (VD) MOS devices.

The development of the model is the result of a lengthy, and also ongoing, research on the HV-MOS devices performed at EPFL with collaboration with other organizations in COMON WG2.

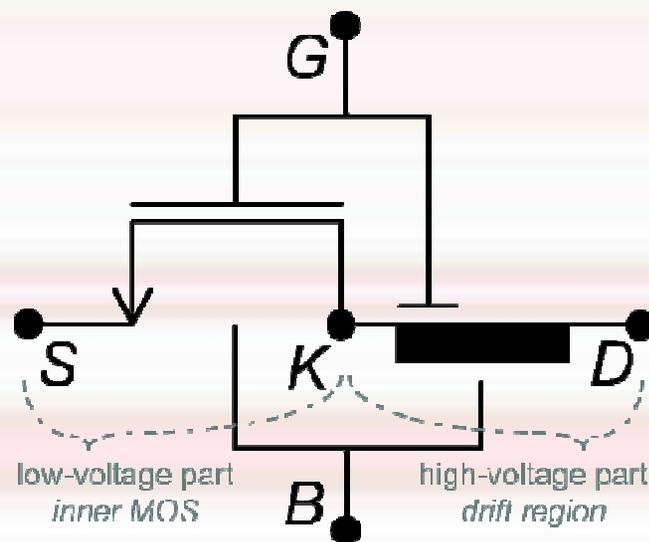
High Voltage MOSFET Modeling

The HV-MOS devices can be analyzed as the in-series combination of two simpler compounds, one for the low-voltage part and one for the high-voltage part



High Voltage MOSFET Modeling

Following this approach a macromodel can be built that will describe the HV-MOS device as a whole. The two parts of the macromodel will be described by two separate compact models.



High Voltage MOSFET Modeling

The inner part is addressed using the EKV compact model for MOSFETs, but incorporating specific effects, such as the lateral non-uniform doping of the channel.

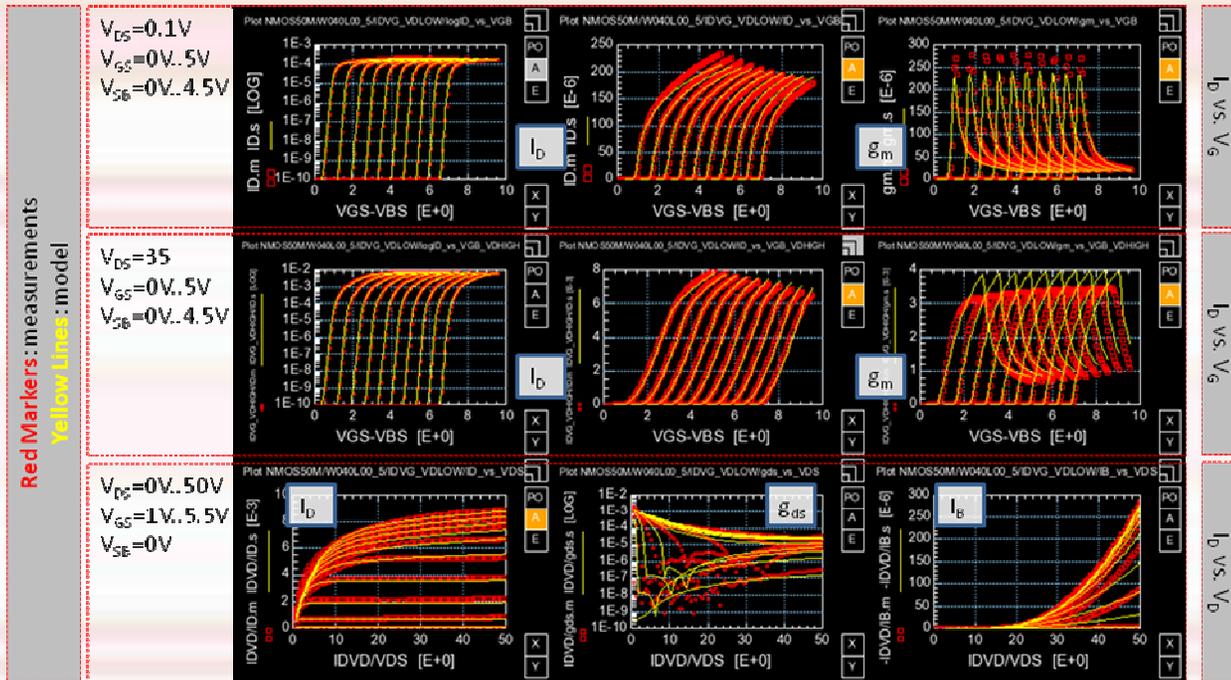
For the high-voltage part of the device a novel physics-based approach has been developed. According to this, the drift region is considered as a single dimensional problem and, with the help of a series of approximations, the system consisting of the Poisson's equation, the drift-diffusion current model and the Boltzmann's equation is managed to be solved analytically with respect to the current

High Voltage MOSFET Modeling

Effects included in the model:

- Laterally non uniform effect (inner MOS)
- Mobility reduction due to vertical field effect
- Quasi-saturation
- First order high field mobility reduction in drift region
- Geometrical small dimension scaling
- Sub-threshold barrier lowering (a.k.a. DIBL)
- Reverse Short Channel Effect
- Channel length modulation
- Temperature effects
- Self-heating effect
- Impact ionization current
- Dynamic Model (capacitances)
- Extrinsic parasitic elements
- Parasitic Junctions

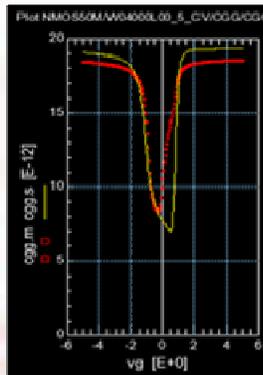
High Voltage MOSFET Modeling



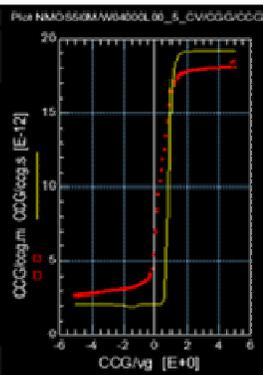
High Voltage MOSFET Modeling

$V_{DS}=0V$
 $V_{GS}=-5V..5V$
 $V_{SB}=0V$

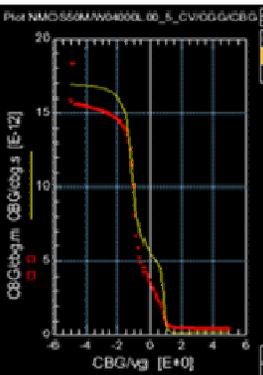
C_{GG} vs. V_G



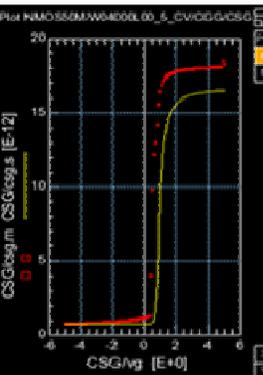
C_{CG} vs. V_G



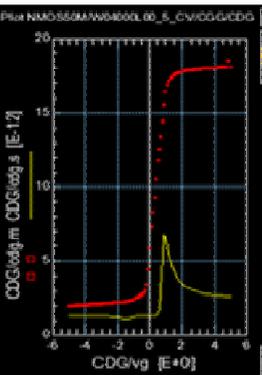
C_{BG} vs. V_G



C_{SG} vs. V_G



C_{DG} vs. V_G



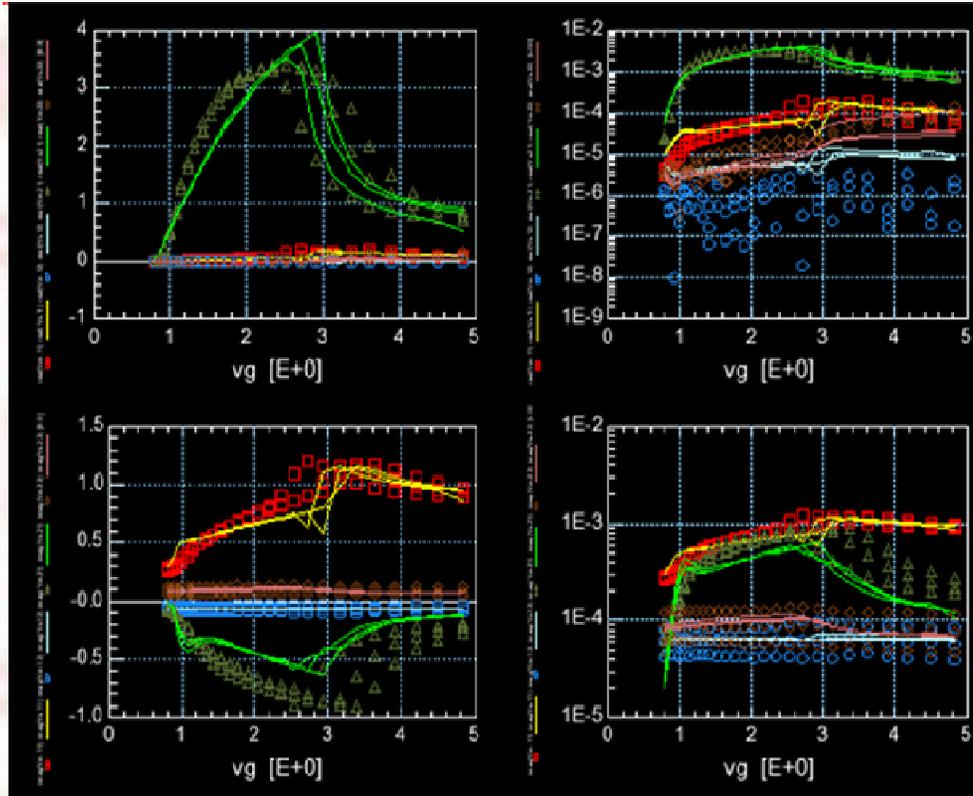
Red Markers: measurements
Yellow Lines: model

High Voltage MOSFET Modeling

$V_{DS}=15V..45V$
 $V_{GS}=0.8V..4V$
 $V_{SB}=0V$
 $Freq=750MHz$

Real

Imag



Linear Scale

Logarithmic Scale

- Real(Y_{11}) - meas
- Real(Y_{11}) - sims
- Real(Y_{12}) - meas
- Real(Y_{12}) - sims
- Real(Y_{21}) - meas
- Real(Y_{21}) - sims
- Real(Y_{22}) - meas
- Real(Y_{22}) - sims

- Imag(Y_{11}) - meas
- Imag(Y_{11}) - sims
- Imag(Y_{12}) - meas
- Imag(Y_{12}) - sims
- Imag(Y_{21}) - meas
- Imag(Y_{21}) - sims
- Imag(Y_{22}) - meas
- Imag(Y_{22}) - sims

HEMT Modeling

Two types of models have been developed by partners:

- 1) A strongly physical model, by UniK
- 2) An empirical model, by TU-Ilmenau

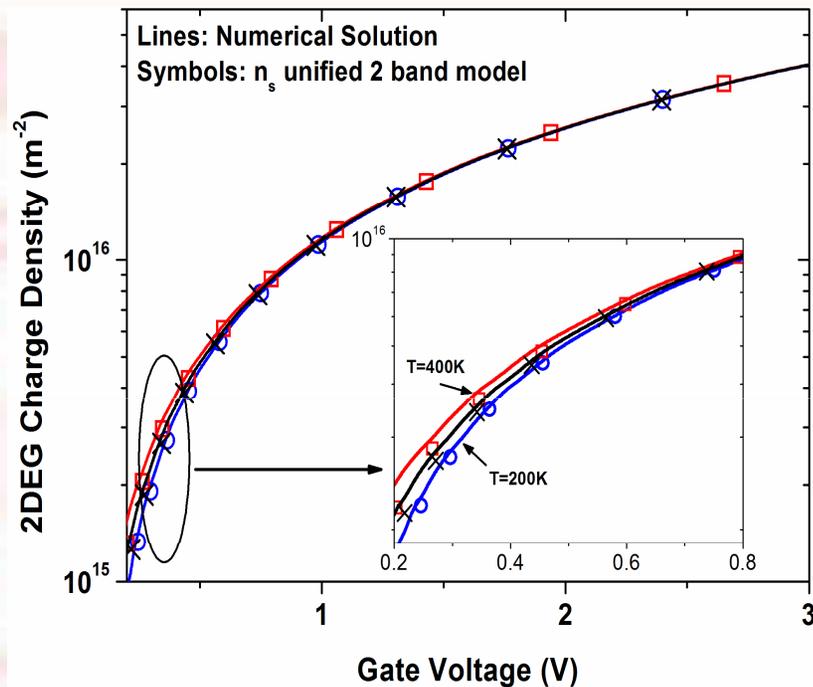
URV developed a high frequency small signal modeling scheme valid for both models

Physically-Based HEMT model

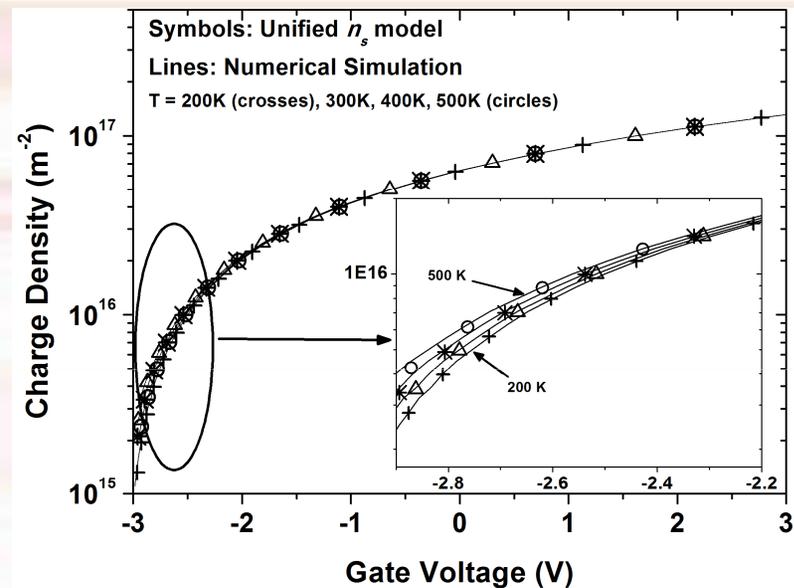
This physical HEMT model is based on an analytical model of the electron gas (2DEG) charge density of these devices

The model has been successfully applied to both GaN and GaAs HEMTs

Physically-Based HEMT model

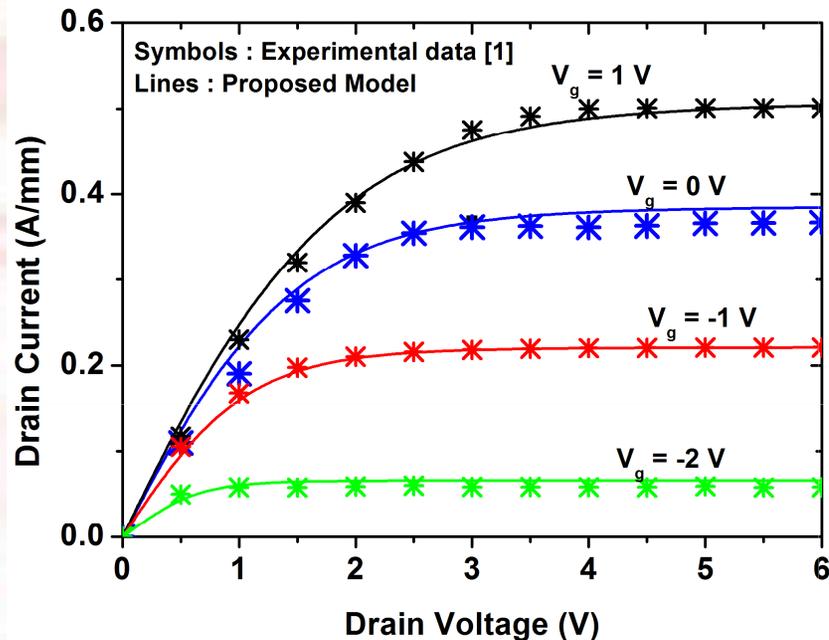


Comparison of numerical calculations and the unified analytical model of n_s versus gate voltage for $T = 200$ K, 300K and 400K for GaAs HEMT devices.



Comparison of numerical calculations and the unified analytical model of n_s versus gate voltage for $T = 200$ K, 300K, 400K and 500K for GaN HEMT devices.

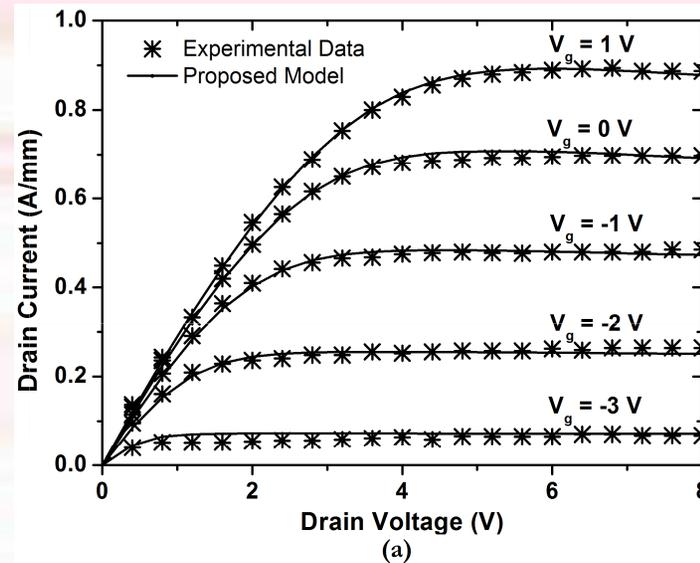
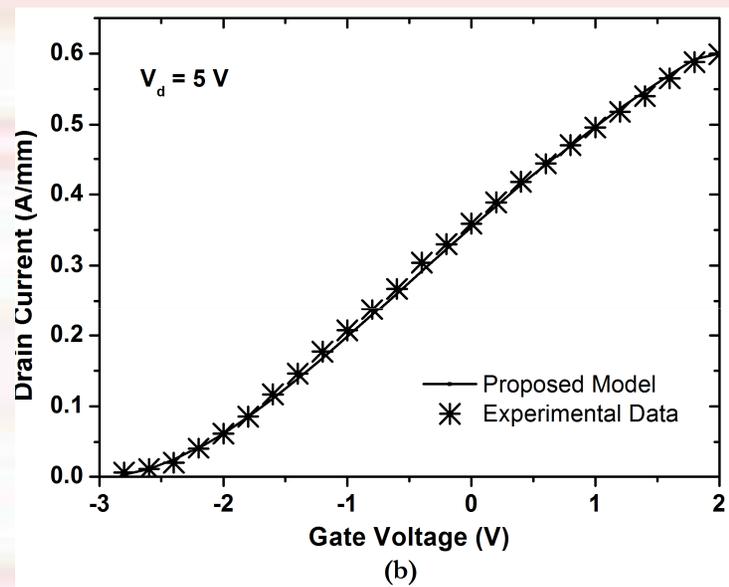
Physically-Based HEMT model



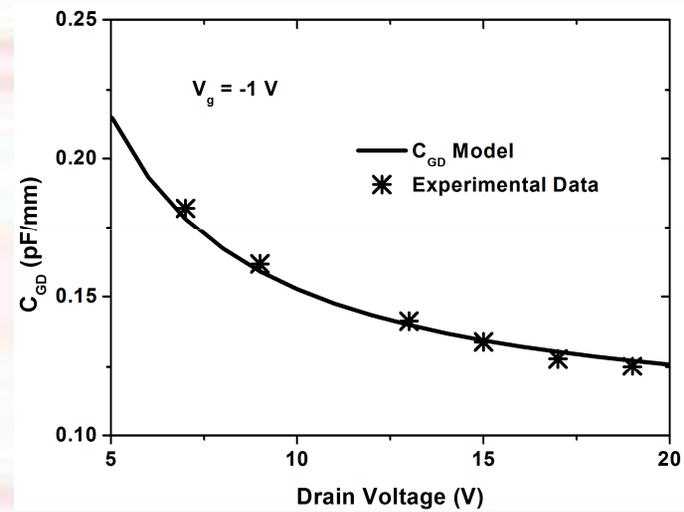
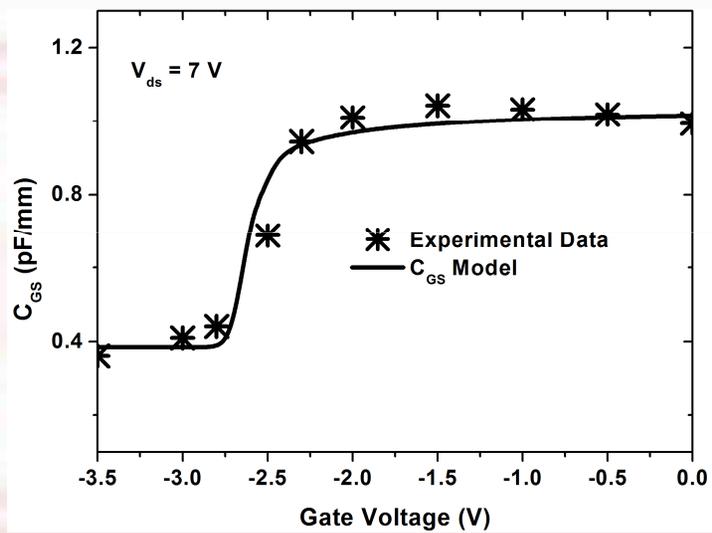
Comparison of proposed drain current model with experimental data from [1] for $L_g = 1\ \mu\text{m}$ device. The simulations are from Verilog-A implementation of model in ELDO simulator.

[1] X. Cheng and Y. Wang., "A Surface-Potential-Based Compact Model for AlGaIn/GaN MODFETs," *IEEE Trans. Electron Devices*, vol. 58, pp. 448-454, February 2011.

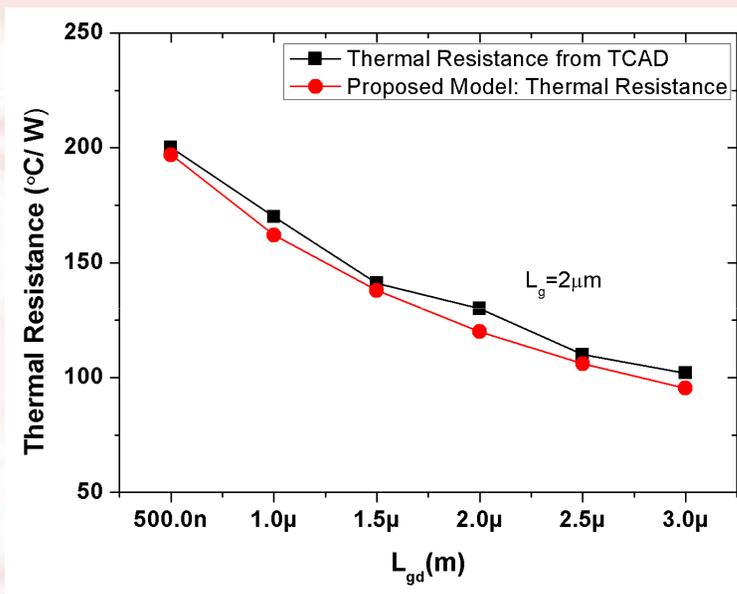
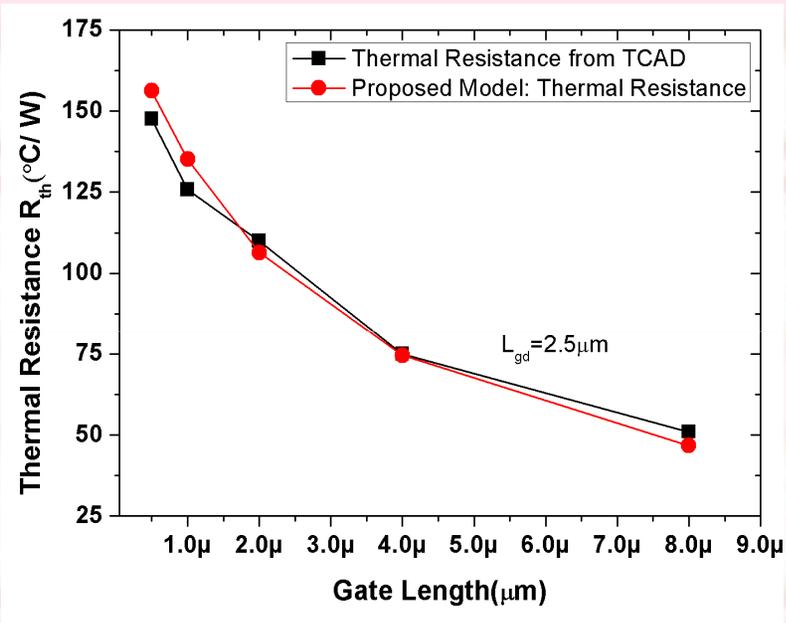
Physically-Based HEMT model



Physically-Based HEMT model



Physically-Based HEMT model



Empirical Compact HEMT Model

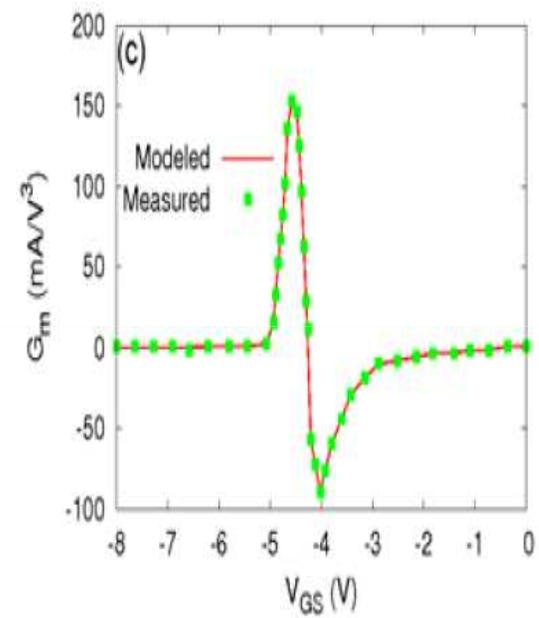
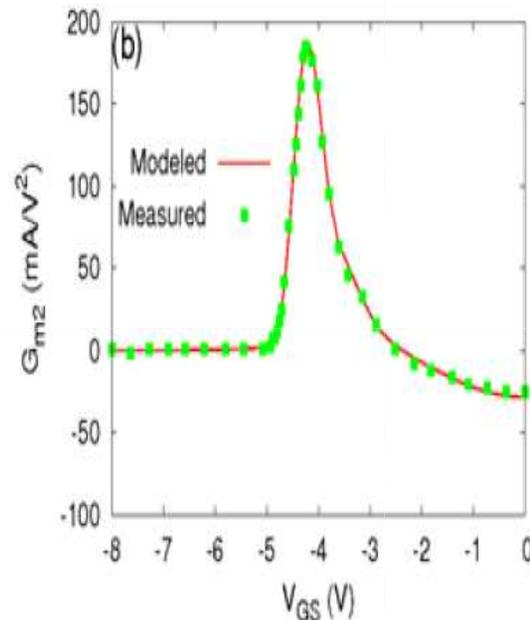
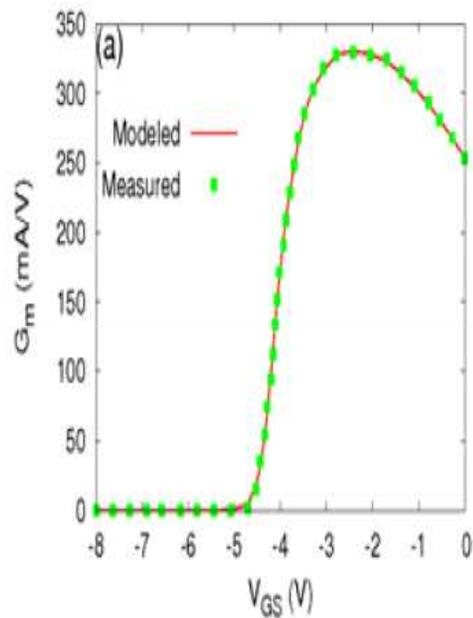
The model has been developed based on the widely used Chalmers model

The model allows an accurate prediction of the $I-V$ characteristics and the corresponding higher-order derivatives, which is necessary for a reliable analysis of intermodulation effects.

It is suitable for the modeling of both low- and high-power devices and accurately includes self-heating effects, while minimizing the cost of parameter fitting.

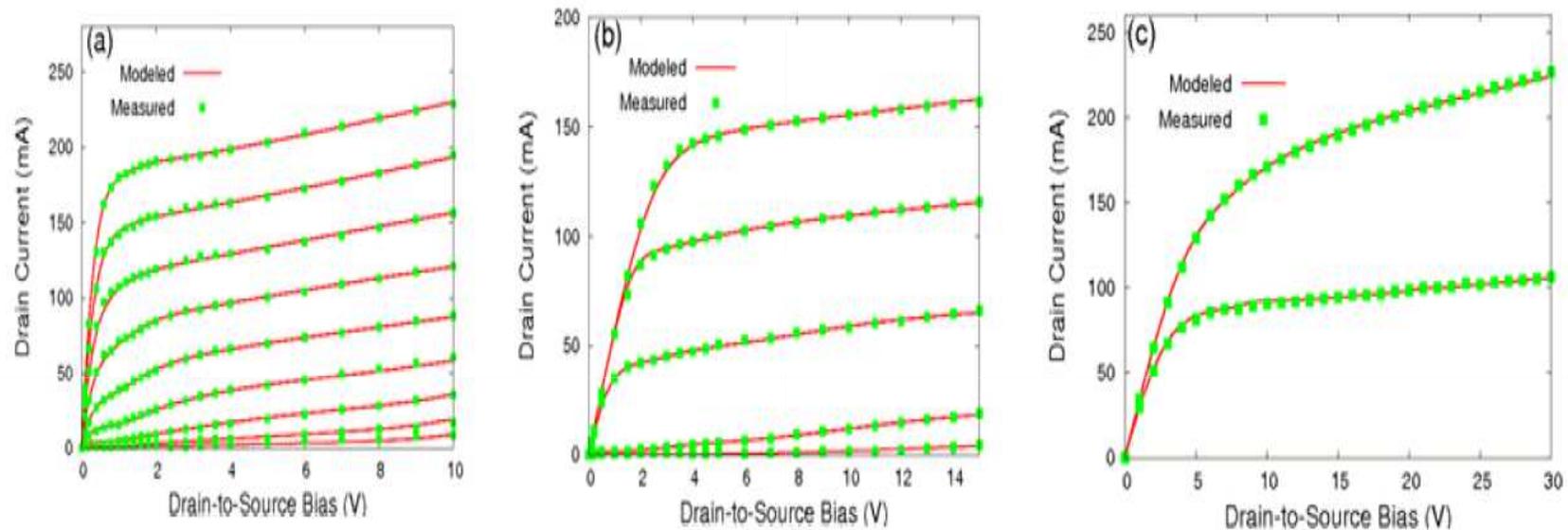
It has been designed to allow an improved flexibility and a simple approach to include self-heating, while guaranteeing continuity and simple extraction procedure.

Empirical Compact HEMT Model



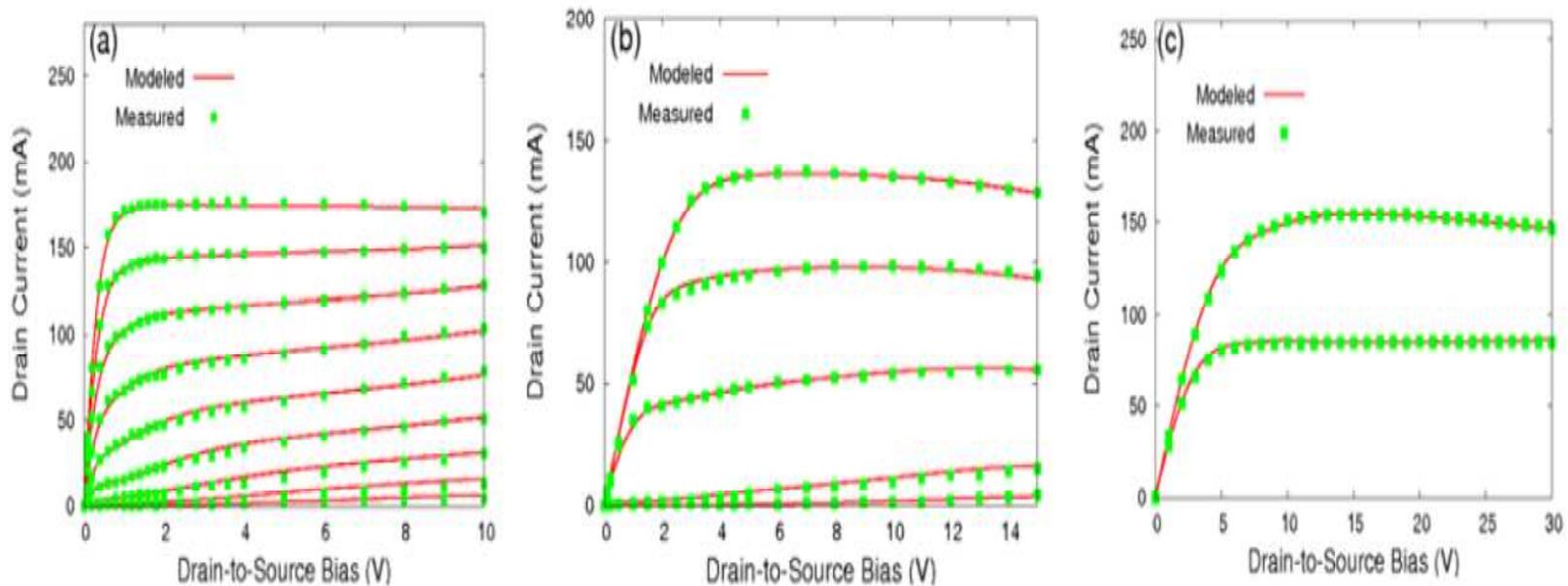
Variation of (a) the transconductance G_m , (b) the first derivative (G_{m2}) and (c) the second derivative (G_{m3}) of the transconductance with gate bias, at $V_{DS} = 6$ V .

Empirical Compact HEMT Model



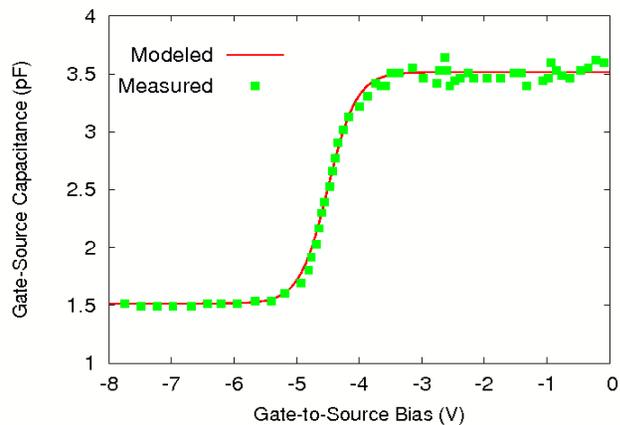
Pulsed $I-V$ characteristics obtained using our newly developed model, for the (a) GaAs pHEMT, (b) the GaN HEMT and (c) the LDMOS device. For the GaAs HEMT, the gate biases are varied over the range of -1.2V to -0.4V with a step of 0.1V . For the GaN HEMT, the gate biases are varied over the range of -4V to 0V with a step of 1V . For the LDMOSFET, the results shown are for gate biases of 3V and 5V .

Empirical Compact HEMT Model

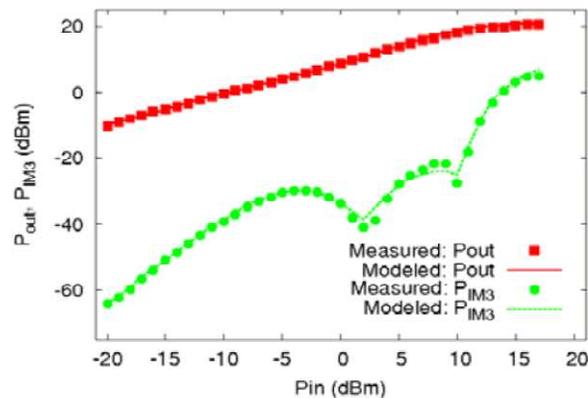
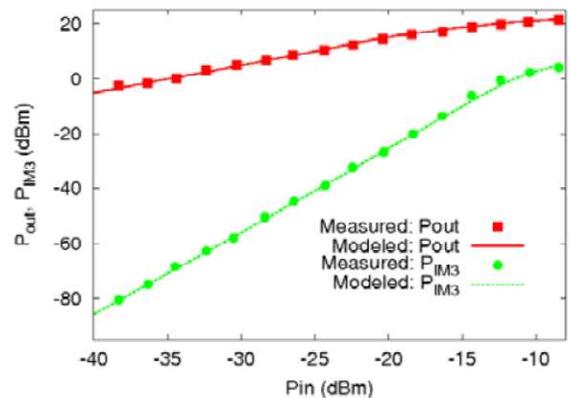


Static DC $I-V$ characteristics, for the (a) GaAs pHEMT, (b) the GaN HEMT and (c) the LDMOS device. For the GaAs HEMT, the gate biases are varied over the range of -1.2V to -0.4V with a step of 0.1V . For the GaN HEMT, the gate biases are varied over the range of -4V to 0V with a step of 1V . For the LDMOSFET, the results shown are for gate biases of 3V and 5V .

Empirical Compact HEMT Model



C_{GS} as a function of VGS for a GaN HEMT_{MT}



Variation of the output power and PIM3 with the input power in the saturation region for (top plot) the GaN HEMT [15] and (bottom plot) the LDMOSFET [16]. The results are for a class A configuration. The GaN HEMT results are obtained at the frequency of 900MHz, at a drain bias of 6V and a gate bias of -3V. The Si LDMOS results are obtained at the frequency of 100MHz, at a drain bias of 20V and a gate bias of 1.3V.

Conclusions



Under the framework of the “COMON” EU Project, compact models for Multi-Gate MOSFETs, HV MOSFETs and HEMTs have been developed.

By the end of “COMON” (Nov 2012) several models will be completed, in Verilog-A codes, and ready for standardization:

- 1) Three Multi-Gate MOSFET models: design-oriented, predictive and mixed predictive design oriented
- 2) One HV MOSFET model
- 3) Two HEMT models for GaAs and GaN HEMTs: one empirical model and one physically-based model

Thank you for your attention!