Poly-Si n+/TiN stack layers obtained by ECR plasmas as metal gate for sub-22 nm CMOS technology

Alisson Garcia, Marcos V. Puydinger dos Santos, José Alexandre Diniz and Jacobus W. Swart.
To keep the CMOS technology on the Roadmap:


This Work: Poly-Si/TiN as metal gate electrode
Problems of Poly Silicon Gate Electrode:

- Boron Penetration;
- High gate resistivity;
- Not compatible with High-\(K\) dielectrics;
- Poly Depletion Effect;

\[
\frac{1}{C_{\text{oxinv}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{poli}}} + \frac{1}{C_{\text{Si}}}
\]
Requirements for metal-gate electrode
new materials:
• Low electrical resistivity < 400 \(\mu\Omega\).cm;
• Thermal stability;
• Compatibility with high-k dielectrics and MOS technology;
• Work Functions between 4.1 eV and 5.1 eV

Our solution: TiN as metal-gate

Poly-Si cap on TiN is used to avoid surface oxidation and to keep thermal stability for process at high temperature (~1000°C) – Poly-Si/TiN can be used in gate first technology

TiN deposition by N$_2$/Ar reactive sputtering

Titanium nitride as promising gate electrode for MOS technology

Lucas P. B. Lima$^{1,2}$, Milena A. Moreira$^{1,2}$, José A. Diniz$^{1,2}$, and Ioshiaki Doi$^{1,2}$

- DC Power: 1000 W;
- N$_2$/Ar ratio: 0.33;

XRD spectra of TiN for different DC power.
Our Previous Work

Structural Analysis: Raman Spectroscopy

Electrical Analysis: C-V and I-V curves

- Metal Work Function
- Flat-band Voltage
- Effective Charge Density

MOS Capacitor

Schottky Diode

• Metal Work Function
• Ideality Factor

C-V curves

Raman Spectroscopy

I-V curves

300 nm

8 nm

300 nm

200 nm

200 nm

n+ Si (100)
Titanium nitride as electrode for MOS technology and Schottky diode: Alternative extraction method of titanium nitride work function

L.P.B. Lima$^{a,b}$, J.A. Diniz$^{a,b,*}$, I. Doi$^{a,b}$, J. Godoy Fo$^b$

$W_F = 4.2$ eV

$W_e = 4.5$ eV

[Normalized Capacitance]

- Sintering Time: 5 minutes
- Sintering Time: 10 minutes

$\text{Bias [V]}$ vs. $\text{Normalized Capacitance}$

$W_e = 4.5$ eV

Reduced distortion with sintering time of 10 min

$[1/\text{slope}]$ to extract the ideality factor, the voltage Schottky barrier and work function
Titanium nitride as electrode for MOS technology and Schottky diode: Alternative extraction method of titanium nitride work function

L.P.B. Lima\textsuperscript{a,b}, J.A. Diniz\textsuperscript{a,b,*}, I. Doi\textsuperscript{a,b}, J. Godoy Fo\textsuperscript{b}

TiN

SiO

TiN

+n-Si (100)

Al

Minimum thickness value of 20 nm

$W_F = 4.2$ eV
This Work

- Gate dielectric
  - Si-p

- Ti
  - Ti deposition E-beam Evaporation 10 Å or 20 Å

- TiN
  - ECR plasma nitridation of Ti layer
    - ECR power = 500W/Pressure = 4 mTorr
    - Temperature: 20°C/Process Time: 20 min
    - Four different gas mixtures:
      1- N2 flow=5sccm/Ar flow=25sccm ;
      2- N2 flow=10sccm/Ar flow=20sccm;
      3- N2 flow=15sccm/Ar flow=15sccm;
      4- N2 flow=20sccm/Ar flow=10sccm.

- ECR-CVD of a-Si:H
  - ECR power = 500W/Pressure = 4 mTorr/
  - Temperature: 20°C/Process Time: 10 min
  - Gas mixtures:
    - SiH4 flow=200sccm/Ar flow=20sccm ;
### This work

8 different TiN films

<table>
<thead>
<tr>
<th>Ti (Å)</th>
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<th>Ar (sccm)</th>
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Names of samples

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8 different TiN films

Requirement for sub-22 nm CMOS technology: TiN thickness must be thinner than 10 nm

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Samples for Physical Characterization (SEM/EDS/Raman):

- RCA clean
- Wet oxidation 1000°C/100 min
  Thickness ~800 nm
- Ti deposition
  E-beam
  Evaporation
  10 Å or 20 Å
- ECR plasma nitridation of Ti layer
- ECR-CVD of amorphous Si layer (a-Si:H)
- Ti deposition
- SiO₂
- Si-p
- TiN
- TiN
- a-Si:H
- SiO₂
- Si-p
- RTA/ 1000°C/60 s/N₂ ambient
- Raman spectroscopy
- Raman spectroscopy + FIB/SEM system:
  Cross section/SEM + EDS
Experiments – MOS capacitors

MOS Capacitors for Electrical Characterization

RCA clean

ECR plasma oxynitridation
Thickness ~5 nm

Ti deposition
E-beam Evaporation
10 Å or 20 Å

ECR plasma nitridation of Ti layer

ECR-CVD of amorphous Si layer (a-Si:H)

Si-p

Si-p

Si-p

Si-p

Si-p

Si-p

Si-p

RTA/1000°C/60 s/N2 ambient

31P+ ion implantation/E=20keV/dose=1015 cm^-2

Poly-Si n+

Poly-Si n+

Poly-Si n+

Poly-Si n+

Poly-Si n+

Si-p

SiOxNy

SiOxNy

SiOxNy

SiOxNy

Si-p

Si-p

Si-p

Si-p

Si-p

Si-p

SiOxNy

SiOxNy

SiOxNy

SiOxNy

SiOxNy

Si-p

SiOxNy

SiOxNy

SiOxNy

Si-p

Al sputtering Deposition + Sintering (30 min) in forming gas

Lithography + etching to define capacitors

Al back side contact

Si-p

Poly-Si n+

TiN

SiOxNy

Si-p

Poly-Si n+

Si-p

Poly-Si n+

SiOxNy

Poly-Si n+

SiOxNy

TiN

SiOxNy

Si-p

SiOxNy

Si-p

Si-p

Si-p

Si-p

Si-p

Si-p

Si-p
After ECR plasma nitridation of Ti layer + RTA

TA and LA modes are related to the vibrations of Ti atoms enclosing N vacancies, indicating Ti rich films.

c- Si from substrate

SAMPLES
Ti10

SAMPLES
Ti20
Results - Raman

after ECR-CVD of amorphous Si layer (a-Si:H)+RTA

Because:
-a-Si: ~480 cm\(^{-1}\).
-c-Si: ~521 cm\(^{-1}\).

LA mode + RTA
Amorphous to crystalline

SAMPLES Ti10

SAMPLES Ti20
Results - SEM

Cross Sections - samples Ti10

Ti10N5Ar25
Thicknes ~6.1 nm

Ti10N15Ar15
Thicknes ~9.8 nm

Ti10N10Ar20
Thicknes ~6.2 nm

Ti10N20Ar10
Thicknes ~18.7 nm
Results - SEM

Cross Sections - samples Ti20

Ti20N5Ar25
Thickness ~7.1 nm

Ti20N10Ar20
Thickness ~11.2 nm

Ti20N15Ar15
Thickness ~13.7 nm

Ti20N20Ar10
Thickness ~8.9 nm
Results - SEM

Error of measurement ~ SEM resolution ~ 3nm

1- For (N2/Ar) ratios up to 1.0, the thickness values are increased with ratio;

2- For (N2/Ar) ratios higher than 1.0, the thickness values are increased and decreased with ratio for films obtained from Ti layers of 1 and 2 nm, respectively;

3- It could be expected that the thickness values would increase with ratio. Thus, the films obtained from Ti layers of 2 nm with ratio of 2.0 must be further investigated.

Thickness values thinner than 10 nm are mandatory requirements for sub-22nm CMOS technology for gate electrodes.
Results – EDS

after ECR-CVD of amorphous Si layer (a-Si:H)+RTA

E = 2 keV

SAMPLES Ti10

Energies which correspond the transitions for Ti and N elements

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<th>elements</th>
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<tr>
<td>Ti10N5Ar25</td>
<td>Ti</td>
<td>0.4; 0.45;</td>
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<tr>
<td></td>
<td>N</td>
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All films have presented Ti and N
Results - EDS

after ECR-CVD of amorphous Si layer (a-Si:H)+RTA

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All films have presented Ti and N
C-V Curves
MOS Capacitors

Normalized Capacitance

Ti10N5Ar25
$V_{FB} = -0.72V$

Ti10N15Ar15
$V_{FB} = -1.1V$

Ti10N20Ar10
$V_{FB} = -3.7V$

Normalized Capacitance

Ti20N10Ar20
$V_{FB} = -0.3V$

Ti20N15Ar15
$V_{FB} = -0.3V$

Ti20N20Ar10
$V_{FB} = -1.1V$
C-V Curves
MOS Capacitors

Suitable for MOS technology
**C-V Curves**

**MOS Capacitors**

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** R. Chau et al, “Application of High-k Gate Dielectrics and Metal Gate Electrodes to enable Silicon and Non-Silicon Logic Nanotechnology” (2005).
### C-V Curves

**MOS Capacitors**

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<tr>
<th>Sample</th>
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<th>Thickness (nm)</th>
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<td>NMOS</td>
<td>6.1</td>
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<td>Mid gap</td>
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<td>Ti20N10Ar20</td>
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<td>Mid gap</td>
<td>11.2</td>
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**Suitable for MOS technology**
C-V Curves
MOS Capacitors

**Normalized Capacitance**

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Suitable for sub-22nm CMOS technology
A new alternative gate first process has been developed, based on ECR plasmas after ultra-thin Ti deposition.
The obtained Poly-Si/TiN structures present:

- From Raman spectroscopy:
  - TiN films present the same structure;
  - a-Si:H became Poly-Si after RTA.
- From SEM and EDS analyses:
  - Thickness values of TiN films are thinner than 20 nm, which is the minimum value obtained by sputtering, and all films present Ti and N elements;
- From C-V curves of MOS capacitor:
  - TiN films are compatible with CMOS technology, can be used as mid-gap electrode and can be obtained in a gate first process.
The authors would like to thank:
- CCS staff for device processing and characterization.
- The work is supported by:

- FAPESP
- CNPq
- CAPES
- NAMITEC