Bringing Device Models Into Production

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Agenda

1. Introduction
2. Spice model from University to simulator
3. Model verification and benchmark
4. Model integration to EDA tools
5. Summary
• Continue device shrinking (Moore’s law)
  – Planar MOSFET
  – Different channel materials
  – Multi-gate device (FinFET, tri-gate)

• More physical effects for small device geometry
  – Substrate leak (HCI)
  – Gate leak
  – GIDL
  – High K material, etc.

• Improve modeling
  – Vth based model
  – Surface potential based model
New Devices Enabling… (Application driven)

- Efficient representation of new devices for
  - RF/wireless application
  - High voltage, high speed, low power, mems
Verification, SPICE Verification Costs Increasing

- Verification costs are… exploding
  - 85% CAGR* first time development
- Semiconductor high market growth – low power
  - Computing (tablet), wireless (mobile), wired (data centers), industrial mil/aero, automotive
- Time to market
  - Increasing design gap
  - Percentage of re-spins projected to almost 50% at 14nm*

* Source: Semico

Semico: Design Cycle Time Increasingly Out of Sync with Market Needs

Time required for design verification exploding – need more time
Design and verification solutions stressed

• Variation increasing
  – 5% per sigma 28nm, 6% per sigma 20nm
  – Critical to determine impact on design

• Exponential growth in design size and complexity
  – Low power architecture, power domains - stretch analysis capacity
  – Continued increased in gate count, functionality

• Resources required for the same coverage increasing over 30%

*Increased complexity, variation explodes simulation time*

Source: Cadence characterization team
SPICE Transient Simulation Activities

• Parse, elaborate and setup the simulation
• Transient Analysis
  For each time-step
    For each iteration {
      – Evaluate each device's I, Q, G & C and Load into the Matrix & RHS
      – Solve the Matrix
    } repeat until the solution converges
    Select the next time-step, to satisfy error constraints
  } repeat until the analysis is complete
• Similar inner loop for most analyses
• Other activities, output, assert, current probing
SPICE Transient Simulation Activities

• Device **evaluation**
  – Majority (70+%) of CPU for small to medium sized designs
  – Device evaluations are independent of each other, opportunities for parallelization

• Matrix **solve**
  – Dominates total CPU for large and/or post-layout designs

• Reduce total number of iterations and removing convergence difficulties is critical
Spice model at university (or model developer)

• Develop model equation for core model
  
  – Vth based model: Formulate model equation
    – Single IV and CV equations for all regions
  
  – Surface based model:
    – simplify and solve Poisson equation
    – Develop IV/CV model
  
  – MOSFET symmetric handling

• Consider various device technologies
  
  – Support high-K dielectric gate
  – Different channel materials
  – Pocket implement
  – ...
Spice model at university (or model developer)

• Develop model for various physical effects
  – Internal source/drain/gate/bulk resistance
  – DIBL
  – NQS
  – Self-heating
  – Layout dependent effect
  – ....

• Develop model for parasitic model
  – Overlap cap
  – Junction
Spice model evaluation (potential user, like CMC member)

- Primarily focus on device behavior
  - Fit TCAD data
  - Fit measured IV/CV data
  - Check device model geometric scaling
  - Check device model temperature dependency
  - Layout effect, self-heating, NQS, etc.

- Spice parameter extraction
  - Is it easy to extract Spice model parameter
Spice model evaluation (potential user, like CMC member)

- Simulator convergence criteria
  - RHS continuous
  - First order derivative continuous
  - Second order derivative

- Most device model
  - RHS continuous
  - No guarantee on first order derivative continuous

- Monotonic
  - IV must be monotonic to avoid multiple solutions
Example of non-monotonic IV

$\text{Id vs Vg}$ DC sweep

$\text{Id vs Vd}$ DC sweep
Examples of model issue

Discontinuity

Discontinuity
Examples of model issue

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<th>V refs</th>
<th>V bdc</th>
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<td>vcp</td>
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**Diagram:**

- **Vb = -0.8, Vc: -10 ~ 0**
- **Vb = -0.8, Vc: 0 ~ -10**
Model enhancement for simulator

- Support various conventional outputs
- Add mfactor, trise
- Support simulation functionality, alter/altergroup, Monte Carlo, etc.
- Support dcmatch analysis
- Etc.
Integrate model to various simulation tools

- Tune model performance and memory usage
- Integrate model into various products
- Consider model parallelization
- Consider model for fast Spice usage
- Etc.
Spice model implementation for simulator

- **Model evaluation**
  - Verilog-A or Spice3 code evaluation
  - Device behavior check as model developer (IV/CV/Temperature/… sweep)
  - Simulation speed comparing to similar device model
    - MOSFET comparing to MOSFET, BJT to BJT, etc.
  - Check memory usage

- **Apple to apple comparison**
  - Extract Spice parameter from the same device IV/CV data
  - Turn on the same physical effects
  - The same feature, like NSQ, self-heating, internal node, etc.
Comparison model A and model B

<table>
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<tr>
<th>Test case</th>
<th># of mosfets</th>
<th>Tran Time (sec)</th>
<th>Iteration #</th>
<th>Time / (#Iter * #Device)</th>
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Comparison model A and model B (normalized with model A)

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## Spectre Comparison of Peak Memory

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Model QA

• Implement device model into simulator, like Spectre
  – Compare simulator device model behavior with original model in Verilog-A or Spice3
  – Complete CMC QA suite
  – Complete company model QA suite (more comprehensive) by R&D
  – Send model to product verification team for fully qualification

• Beta or EAP release
  – Beta test for foundry, potential

• Official release
Minimizing Production Impact

- Accuracy, performance and capacity
  - Converge, converge, converge

- Qualify early and for each functional, device and cost
  - Prototype models
  - Foundry model qualification – where programs exist
    - Device level
    - Circuit level
  - Partner with companies/teams developing designs

Qualification complete with the real designs
Compromise between Accuracy and Performance

- **errpreset** is a Spectre invention that relieves user from manual tweaking
  - Liberal mode provides satisfies most analog circuit simulation needs
  - Moderate most widely used mode
  - The conservative mode provides the ultimate golden accuracy

<table>
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<th>errpreset</th>
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Integration into various tools

Spectre® Simulation Solution

- Model is the foundation of circuit simulation
- Circuit simulation is the foundation for…
- Integration of SPICE into all other applications comes next
  - EM/IR, Litho electrical analysis, static timing, SoC power analysis, board and signal integrity, standard cell and memory characterization, mixed signal and finally electrically aware design
Making a successful Spice model

- It is not enough even simulator does everything for a device model

- What is needed else
  - Spice model has to be attractive (designer wants to use it)
  - Foundry needs to provide Spice model library
  - Spice model has to qualified for real circuit
    - Convergence (usually more non-convergence shows up)
    - Speed
    - Memory usage
Bring a model to industry

• Procedure
  – University / model developer
  – EDA simulator implementation
  – Foundry provide model library
  – Design likes to use it

• A successful Spice model
  – Must converge
  – Good performance
  – Reasonable memory usage
  – Simulator/Foundry/Designer