Compact Model Coalition

Keith Green (TI)
Chair
Charter

To promote the international, nonexclusive standardization of compact model formulations and the model interfaces.
History and Purpose

• The CMC was formed in 1996 as a collaboration of foundries, fabless companies, IDMs and EDA vendors.

  - Foundry or IDM's Fab → Commercial or In-House Circuit Simulator → Fabless or IDM IC Designer

• Compact models provide the connections.

• Standard compact models enable efficiencies in this process.
## Members

<table>
<thead>
<tr>
<th>Agilent</th>
<th>AIST</th>
<th>Altera</th>
<th>Analog Devices</th>
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<td>Broadcom</td>
<td>Cadence</td>
<td>Denso</td>
<td>Fujitsu Semiconductor</td>
<td>Global Foundries</td>
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<td>IBM</td>
<td>Infineon</td>
<td>Intel</td>
<td>LEAP</td>
<td>LSI Corporation</td>
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<td>Mentor Graphics</td>
<td>Micron</td>
<td>NXP</td>
<td>Panasonic</td>
<td>Peregrine Semi</td>
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<td>ProPlus</td>
<td>Qualcomm</td>
<td>Renesas Electronics</td>
<td>Ricoh</td>
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<td>Silvaco</td>
<td>SK Hynix</td>
<td>Sony</td>
<td>STARC</td>
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<td>Synopsys</td>
<td>TI</td>
<td>Toshiba</td>
<td>Toyota</td>
<td>TSMC</td>
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<td>UMC</td>
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Presently 36 member companies.
Officers

Chair: Keith Green, Texas Instruments
Vice Chair: Peter Lee, Micron
Treasurer: Yoshiharu Furui, Silvaco
Secretary: Kunihiro Sakamoto, AIST
Vision

• Standardized compact models for all major technologies so that customer communication and efficiency can be enhanced.

• Standard interfaces so that models can be tested faster and implemented easier.

• Better compact models for the latest technologies, allowing leading edge design development cycles to shorten.
Strategy

• Examine, promote and standardize compact modeling efforts based upon business needs.

• Encourage developers to dwell on current and near-term problems that will advance compact modeling.

• Provide industry resources for monitoring/mentoring compact model development.

• Provide a standardization process to the compact model developers.
Operations

- Through balloting Working Groups are initiated to develop new standards.
- Working Groups conduct business via teleconferences, email and at quarterly face-to-face CMC meetings.

- CMC quarterly face-to-face meetings:
  - Forum for face-to-face Working Group meetings.
  - Review progress of Working Groups
  - Updates on EDA-member’s status/plans for implementing CMC standards.
  - Coalition-level discussions & decisions
Operations

• A rigorous four-phase process for standards development.
  ➢ Detailed requirements list
  ➢ Search for candidates
  ➢ Member testing
  ➢ Voting processes

• Established standards continue to have Working Groups that drive enhancements and support.

• Model Quality Assurance & Release procedures guide implementation accuracy and code versioning.
Operations

• Some standards are supported at universities funded by member dues.

• Members’ dues are linked to the standards they designate. Designations…
  ➢ Determine funding amounts to Universities
  ➢ Provide access to standard model beta codes
  ➢ Are rights to participate in work-list prioritization decisions
# Working Groups

<table>
<thead>
<tr>
<th>Working Group</th>
<th>Representative</th>
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<tr>
<td>BSIM-Bulk</td>
<td>Kaiman Chan (TI)</td>
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<td>BSIM-SOI</td>
<td>Richard Williams (IBM)</td>
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<td>BSIM-CMG</td>
<td>Richard Williams (IBM)</td>
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<td>Diode Reverse Recovery</td>
<td>Klaus-Willi Pieper (Infineon)</td>
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<td>ET-SOI</td>
<td>Richard Williams (IBM)</td>
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<td>GaN HEMT</td>
<td>Samuel Mertens (Agilent)</td>
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<td>HICUM</td>
<td>Didier Celi (ST)</td>
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<td>HiSIM2</td>
<td>Shigetaka Kumashiro (Renesas)</td>
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<tr>
<td>HiSIM-HV</td>
<td>Ehrenfried Seebacher (ams) &amp; Yoshinori Ueda (Ricoh)</td>
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<tr>
<td>HiSIM-SOI</td>
<td>Kunihiro Sakamoto (AIST)</td>
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<td>MEXTRAM</td>
<td>Jin Tang (TI)</td>
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<tr>
<td>Model QA &amp; Release</td>
<td>Shahriar Moinian (LSI)</td>
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<td>MOSVAR</td>
<td>Geoffrey Coram (ADI)</td>
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<td>Pre-layout Parasitics</td>
<td>Lixin Ge (Qualcomm)</td>
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<td>PSP</td>
<td>Andries Scholten (NXP)</td>
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<td>Reliability</td>
<td>Ahmed Ramadan (Mentor Graphics)</td>
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<td>Standard Operating Point Variables</td>
<td>Samuel Mertens (Agilent)</td>
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<td>Standard SPICE Language</td>
<td>Samuel Mertens (Agilent)</td>
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<td>TMI2</td>
<td>Sandeep Sasargod (Agilent)</td>
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<tr>
<td>Verilog-A Recommended Best Practices</td>
<td>Geoffrey Coram (ADI)</td>
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University Partners

- University of California at Berkeley – Professor Chenming Hu
  - BSIM3, BSIM4, BSIM6, BSIM-SOI and BSIM-CMG

- Hiroshima University – Professor Mitiko Miura-Mattausch
  - HiSIM2, HiSIM_HV and HiSIM-SOI

- Delft University of Technology – Professor Ramses van der Toorn
  - MEXTRAM and PSP

- University of California at San Diego – Professor Michael Schroter
  - HICUM
Compact Models:

- Planar Bulk MOSFETs:
  - BSIM3 (1995)
  - BSIM4 (2000)
  - BSIM6 (2013)
  - PSP (2006)
  - HiSIM2 (2011)

- LDMOS:
  - HiSIM_HV (2007)

- SOI MOSFETs:
  - BSIMSOI (2002)
  - HiSIM-SOI (2012)

- BJTs:
  - HICUM (2004)

- Multi-Gate MOSFETs:
  - BSIM-CMG (2012)

- MOS Varactor:
  - MOSVAR (2006)

- Resistors:
  - R2_CMC (2005)
  - R3_CMC (2007)

- Junction Diodes:
  - DIODE_CMC (2009)

Other Standards:

- TMI2 Modeling API (2010)
- Standard SPICE Language (2012)
Works In Progress

• ET-SOI Model Standard
  14nm → 10nm CMOS

• GaN HEMT Model Standard
  Power & RF

• Reliability Modeling API Standard
  CHC, NBTI, PBTI, …
Member Benefits

• **Members have a say** in what models become a standard.

• **Members** have the opportunity to request enhancements specific to their needs.

• **Members attend** quarterly CMC meetings with leading industry and academic model developers, where they learn about technology, often before they are published in the literature.

• **Members have access** to model beta codes.

• **Members have access** to resistor, varactor and diode model codes.

• All of the information from the meetings is available to **members only** on the CMC website.
Move to Si2: “CMC 2.0”

• For the first time in its 17-year history the CMC is partnered with an organization that is dedicated to developing EDA standards.

• Expected enhancements:
  ➢ Broader impact through synergies with other Si2 coalitions
  ➢ Improved website and documentation
  ➢ More visibility via Si2’s channels for marketing and publicity
  ➢ Increased operational efficiency
Summary

• The CMC enhances the IC development process
  – Standardizing high-quality device models and simulator interfaces.
  – Providing a forum and mechanism to keep these standards current to industry needs.

• The CMC is a member-driven organization open to any company in the semiconductor business.