TCAD in the more Moore and more than Moore era

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Overview

• Nanoelectronic Device Simulations
  From Moore’s Law to TCAD
• Simulation Approach and Validation
  Model choice and validation
• Application to Nanoscale Devices
  Self-heating in NWFETs
  Metal-dichalcogenide FETs
• Outlook and Conclusion
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Motivation: Future of Moore’s Scaling Law

The transistor evolution is governed by Moore’s Scaling Law

- 65nm (2005)
- 45nm (2007)
- 32nm (2009)
- 22nm (2011)
- XXnm (2020)

Every 18-24 months, 30% dimension scaling. ⇒ area is divided by 2.

Breakthrough: 2D->3D
New Structures

Nanowire
P. Hashemi et al., *EDL* 30, 401 (2009)

3-Gate SOI
Next Generation Devices

Graphene

CNT
Supratik Guha, IBM Research

III-V UTB
Y.Q. Wu et al., *EDL* 30, 700 (2009)

MoS$_2$

Ge UTB
R. Zhang et al., *TED* 59, 335 (2012)

New Materials
Next Generation Devices

New Concepts

NEMS

SET

BTB Tunneling
W.Y. Choi et al., EDL 28, 743 (2007)

Advanced Design Tool(s) Required
TCAD Tool Requirements

Three different perspectives: EE+PHYS+HPC

Device Engineering

- **Industrial-Strength** Nano-electronic Device Simulator
- **Multi-Geometry** Capabilities
- Explore, Understand, Predict, Optimize Novel Designs

Physical Models

- 3D **Quantum** Transport Solver
- Accurate Representation of the Semiconductor Properties
- Atomistic Description of Devices
- **Multi-Physics** Modeling

OMEN

- Accelerate Simulation Time
- Investigate New Phenomena at the Nanometer Scale
- Move Hero Experiments to a Day-to-Day Basis

Efficient Parallel Computing

- \( I_d - V_{gs} \)
- \( p\text{-FET} \) vs. \( n\text{-FET} \)
- Electron Density
- Parallelization Scheme
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Requirements for the simulation approach

Conventional approach: **drift-diffusion** (DD) simulator

\[
\begin{align*}
\vec{J}_n &= q \cdot n \cdot \mu_n \cdot \vec{E} + q \cdot D_n \cdot \nabla n \\
\vec{J}_p &= q \cdot p \cdot \mu_p \cdot \vec{E} - q \cdot D_p \cdot \nabla p
\end{align*}
\]

DD does not capture **bandstructure** and **confinement** effects

**What is needed**: solution of **Schrödinger** equation (NEGF)

\[
(E - H(k) - \Sigma^R(E,k)) \cdot G^R(E,k) = I
\]

\[
G^<(E,k) = G^R(E,k) \cdot \Sigma^<(E,k) \cdot G^A(E,k)
\]

**Key Component** of NEGF equations

\[H(r,k)\]: Hamiltonian matrix in selected basis (EMA, TB, DFT)
Empirical Nearest-Neighbor **Tight-Binding** Method

**GOOD:**
- bulk CB and VB fitted
- extension to nanostructures
- atomistic description

**BAD:**
- high computational effort
- empirical parametrization

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**Si Electron Bandstructure**

![Si Electron Bandstructure Diagram](image)
Model Validation: III-V HEMT Simulations

Expt: J. del Alamo @ MIT

Thermionic Current over a Potential Barrier

\[ \text{Simulation domain} \]

\[ \text{Simulation} \]

\[ \text{Simulation} \]

\[ \text{Simulation} \]

\[ \text{Experiment} \]

\[ \text{Experiment} \]

\[ \text{Experiment} \]
Model Validation: CNT FET Simulations

Expt: A. Franklin @ IBM YH

Simulation domain

L_g = 9nm

Ambipolar Current Flow

CB

E_f l

E_f r

Source

Drain

V_{ds} = -0.40 V

V_{ds} = -0.01 V

I_d - V_{gs} Characteristics

Experiment

Simulation

x (nm)

E (eV)

Source

Drain

HfO_2

Gate

Air

Simulation domain

 Drain

Source

CB

E_f l

E_f r

Ambipolar Current Flow

V_B
Model Validation: Hetero-BTBT Diode Simulations

Expt: S. Rommel @ RIT SEMATECH
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Objective:
• Explore the scaling behavior of gate-all-around nanowire transistors for sub-10 nm gate length applications, especially *electro-thermal* effects.

Approach:
• Tight-binding \(sp^3d^5s^*\) description of the electron/hole properties
• Quantum transport with *NEGF*
• Ballistic simulations and inclusion of electron-phonon scattering with out-of-equilibrium phonons.

Results and impact:
• Influence of electron-phonon scattering on the nano-device performance: current decrease, and temperature increase.
**Goal:** atomistic simulation of Si gate-all-around NWFET

\[ x = \langle 100 \rangle \]

**e-bandstructure**

\[ m^* = 0.29m_0 \]

**ph-bandstructure**

**Transfer characteristics** \( I_d - V_{gs} \)
**Goal:** atomistic simulation of Si gate-all-around NWFET

$x=<100>$

**Transfer characteristics $I_d-V_{gs}$**

- Uncoupled Scatt.
- Coupled Scatt.
**Objective:**

- Explore the potential of metal-dichalcogenides as logic switches.

**Question:** Can they beat Si?

**Approach:**

- *Ab-initio* modeling of the band-structure properties with VASP
- Projection into Wannier basis
- Quantum transport with NEGF
- Simulations beyond the ballistic limit

**Results and impact:**

- Full-band and scattering important
- Mobility increases with # layers, but electrostatics degrades
- Lower performance than s-Si and III-V semiconductors as FET

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B. Radisavljevic et al. Nat. Nano. 6, 147 (2011)
Ballistic device Simulation

Device specifications:
- Gate length $L_G = 10.7$ nm
- S/D extension $L_S = L_D = 15$ nm
- Supply voltage $V_{DD} = 0.68$ V
- EOT = 0.58 nm
- Doping $N_D = 6 \times 10^{13}$ cm$^{-2}$

NDR observed:
- Where does it come from?
- Is it physical?
- If no, how can we get rid of it
Device simulation with scattering

With electron-phonon scattering:

- $\frac{I_{\text{diss}}}{I_{\text{ball}}}$ current ratio decreases with $V_{gs}$ for $V_{ds} = 0.05$ V due to backscattering
- Ratio increases at $V_{ds} = 0.68$ V because scattering connects narrow bands
Performance comparison with s-Si and InGaAs

- Single-layer MoS$_2$
- s-Si/InGaAs

**MoS$_2$:**
- Good electrostatics control
- Higher m* \(\Rightarrow\) lower v$_{\text{inj}}$
  \(\Rightarrow\) lower ON current
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Conclusion

• **Future of Moore’s Law**
  TCAD to accelerate nano-device innovation

• **Proposed Simulation Approach**
  Good agreement with experimental data
  Dedicated to large variety of nanoscale devices
  Necessity to go beyond $m^*$ and ballistic in MoS$_2$

• **Future Work and Challenges**
  More *ab-initio* device simulations
  Work more closely with experimental groups