gnucap

• What is it?
  – At the beginning
  – What it has become
  – Work in progress
At the beginning

- “ACS” 1990, GPL 1992
- Spice accurate fast spice
- Single engine mixed signal
- Auto insertion of connect modules
SPICE accurate fast spice

• Start with Spice algorithms
• Low rank update, partial solution
• Queues
  – Evaluate, load, review
• Much faster for large circuits
• Better step control
  – Cross events, curve fitting
Mixed signal

- Discrete states, event queue
- Not just analog models of gates!
- Not “relaxation”
- First single engine spice accurate
Auto connect modules

- 1992 GPL
- Smart node has analog and digital properties
- But is primarily one or the other
- Multiple architectures for an entity
- Predates Verilog-A or VHDL-A
Gnucap: has become

- C++
- Early model compiler, pre Verilog-A
- Plugins
- Stable, well tested library
- Formal testing, formal methods in software engineering
Plugins

- Reduce need for forks
- Code quality
  - How to make available unfinished contributions?
  - Too open commits to core is a time bomb
Plugins

- Required
- Shared object files
- Stable well tested library
- “wrappers” enable use of foreign code
  - Spice “C” models (several versions)
Plugins

- Models
- Algorithms
- Commands
- Post-processing
- Measurements
- Languages
- Probes
In progress

- ADMS (not going well)
- GEDA, Qucs interface
- More user-friendly plugin loading
- Verilog Modelgen model compiler
- Schematic and layout file exchange
What's wrong with ADMS

- I can't get into XML
  - Or JSON, or any text markup language
  - Need a real programming language (C++)
- Discrete state devices
- Non-spice architecture
- Connect modules
- Cross events
- Optimization
Plugin interface

- Now: “load” an .so
- Working on: auto “JIT” compile
- Development environment for models, etc.
Verilog-modelgen

- Based on old modelgen
- Put aside hoping for ADMS, now bringing back
- Modular C++
File exchange

• Geda, qucs, ……
• Their formats are polygons
• Use a netlist format, augmented
• Layout vs schematic
• Post-layout simulation
• Based on structural subset of Verilog-AMS