SIMIT

Performance analysis and modeling of 22nm FDSOI MOSFETs

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Outline

- 22nm FDSOI Process Introduction
- FDSOI VS BULK
- Body Biasing in FDSOI
- Learn about Self-Heating Effect (SHE)
- 22nm FDSOI SPICE Model
- Summary

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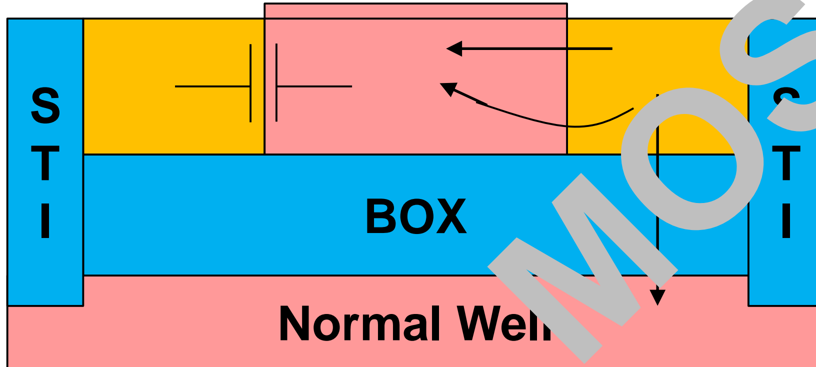
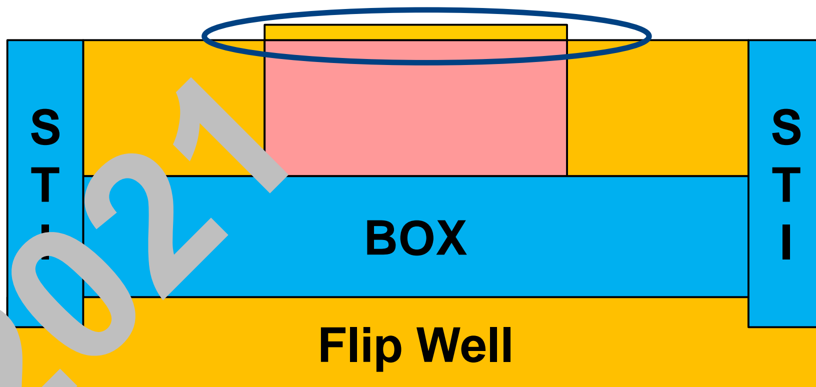
22nm FDSOI Process



Front gate work function modulation



Well engineering

- **High speed**
  - -High mobility
  - -Less parasitic capacitor
- **Power sufficient**
  - -Steeper subthreshold swing
  - -Less junction
  - -Less DIBL
- **Less process variation**
  - -Light doping (RDF)
  - -Flexible Vt option
  - -High integration

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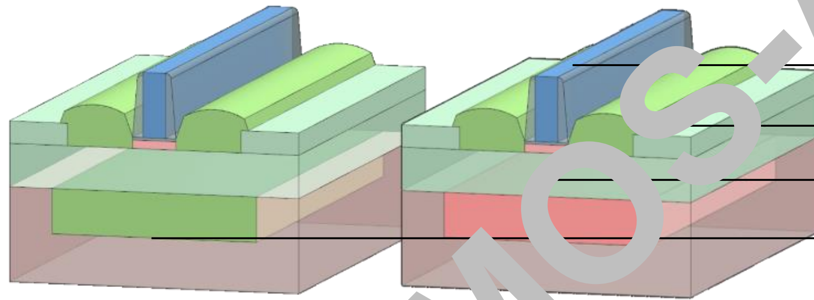
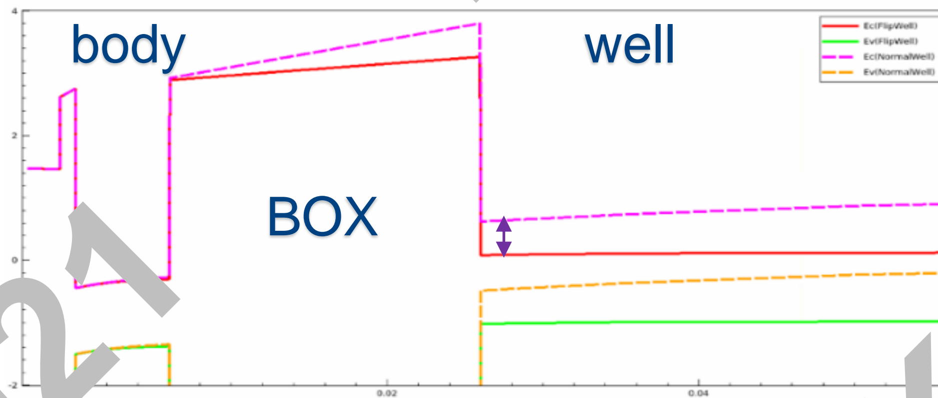
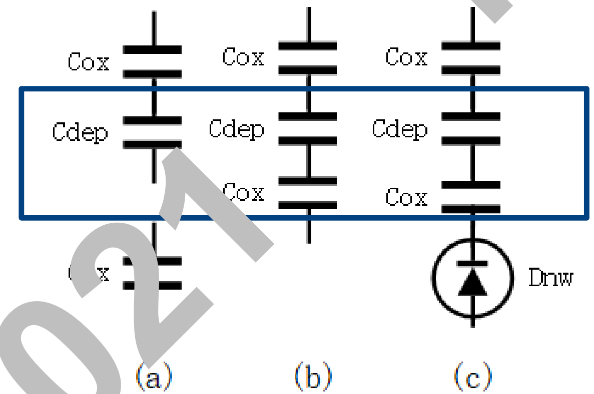
22nm FDSOI Process



- HKMG
- Raised source and drain
- Ultra thin body and box
- Flip well





(a) PDSOI
(b) FDSOI with flip well
(c) FDSOI with normal well

Flip well provides a lower vth option

Steeper SS

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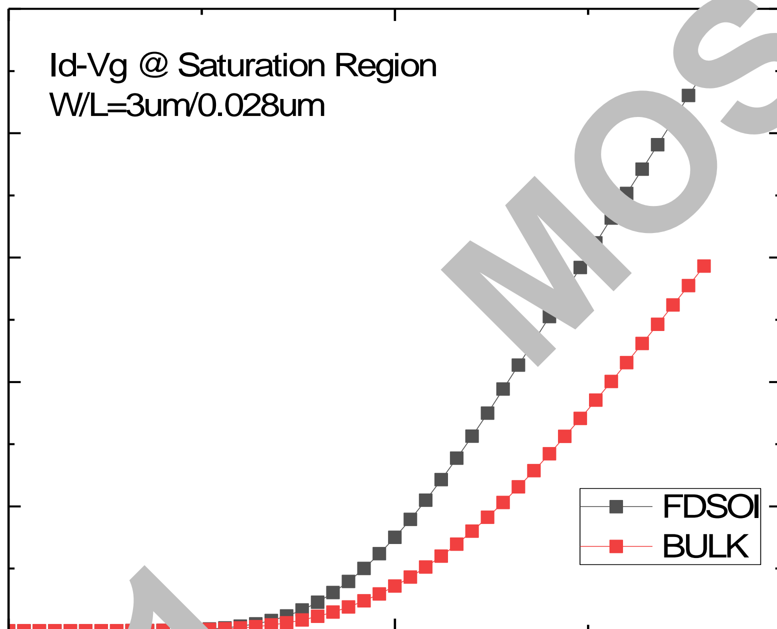
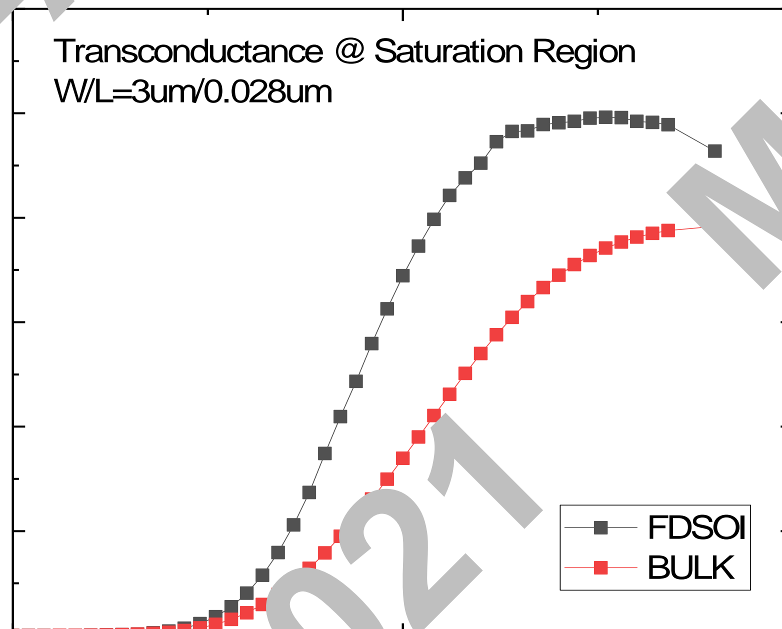
FDSOI VS BULK





Key operation point summary

Process	SS	Ion/Ioff	DIBL	Gmmax
22nm FDSOI	~75mV	4[illegible]5	13.4	4.99mS
28nm BULK	~85mV	1.2[illegible]5	39.2	3.75mS

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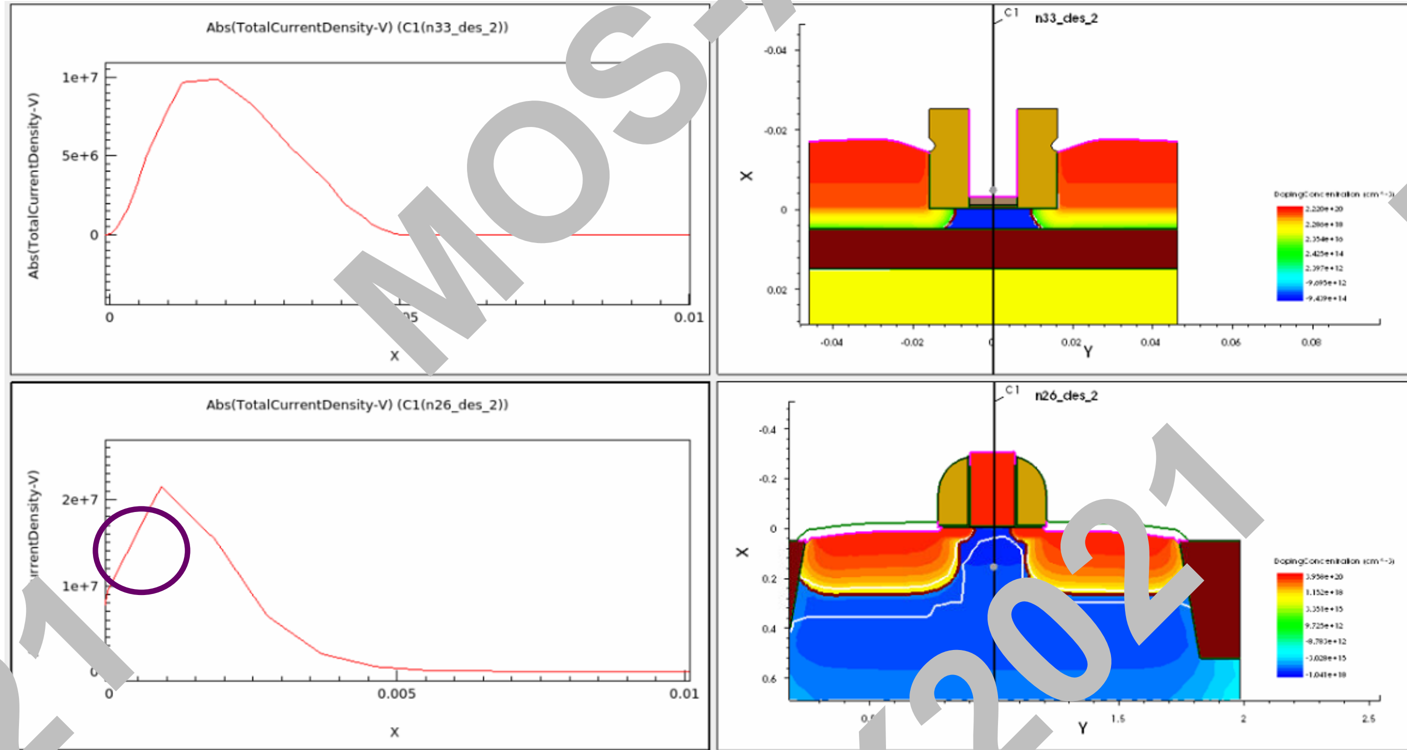
FDSOI VS BULK

Volume Inversion



Surface scattering

The volume inversion increases the mobility in FDSOI devices.

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Body Bias

N type
P type

NMOS
PMOS

S T I | BOX | S T I | BOX | S T I

Flip Well
Normal Well
Psub

Device	NMOSNW	PMOSNW	NMOSFW	PMOSFW
FBB	(0,0.2)	(-0.2,0)	(0,Vdd)	(-Vdd,0)
RBB	(-Vdd,0)	(0,Vdd)	(-0.2,0)	(0,0.2)

Fast speed

Power sufficient

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Body Bias

Plot VS/BULK/IdVg/IdVg_Vs

Plot VS/BULK/IdVg/IdVg_Vs

Plot VS/BULK/IdVg/vth_vs

Plot VS/BULK/IdVb/IdVb_Vs

- In BULK process, depletion layer thickness can be affected by body bias.

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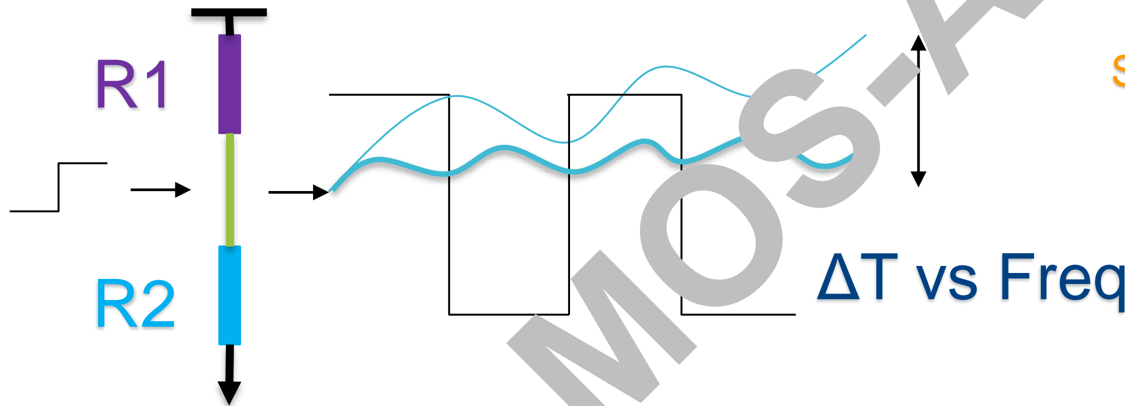
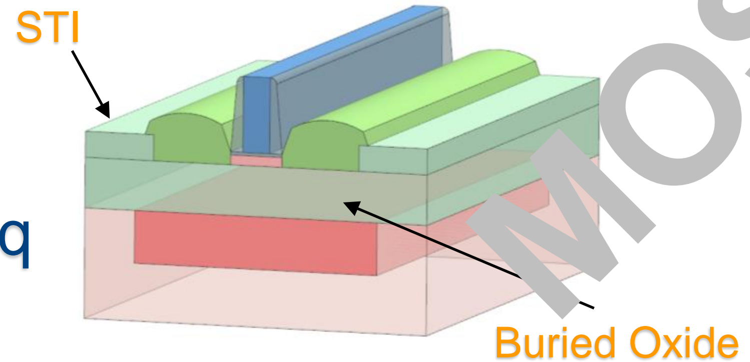
Self-Heating Effect (SHE)



High frequency reduces self-heating effect



Sandwich structure in FDSOI

$$\Delta T = P_{th} * Z_{th} = \frac{I * V}{G_{th} + jwC_{th}}$$

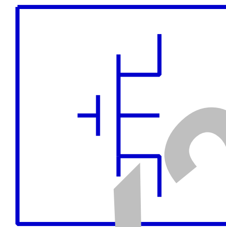
Low Frequency:

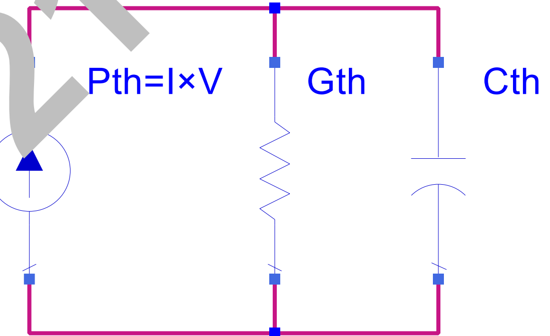
$$\Delta T = I * V * R_{th}$$

High Frequency:

$$\Delta T \approx 0$$

Self-heating free at high frequency
Typically >50Mhz





Equivalent Circuit

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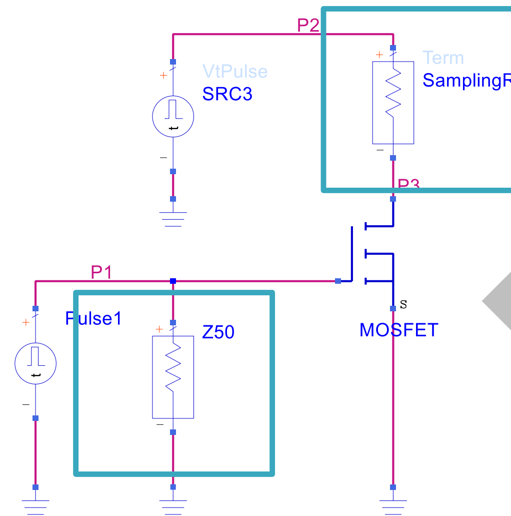
SHE in real device (I)

DC Sweep Data

Real Data



Pulsed IV
(Sampling time dependent)

Disadvantage:

- Complicated measurement setting
- High resolution sampling resistor
- Noise / impedance mismatch

Self-heating effect could be observed in pulse measurement.

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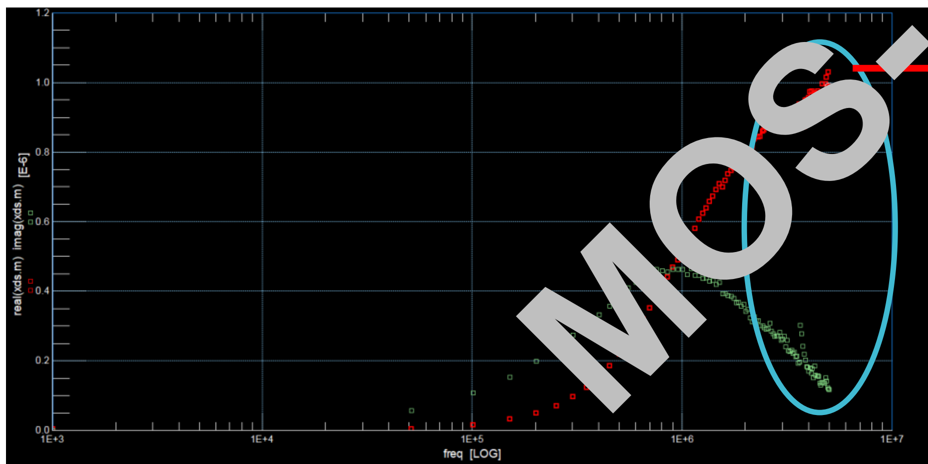
SHE in real device (II)

Realistic Gds vs freq **@Saturation Region**



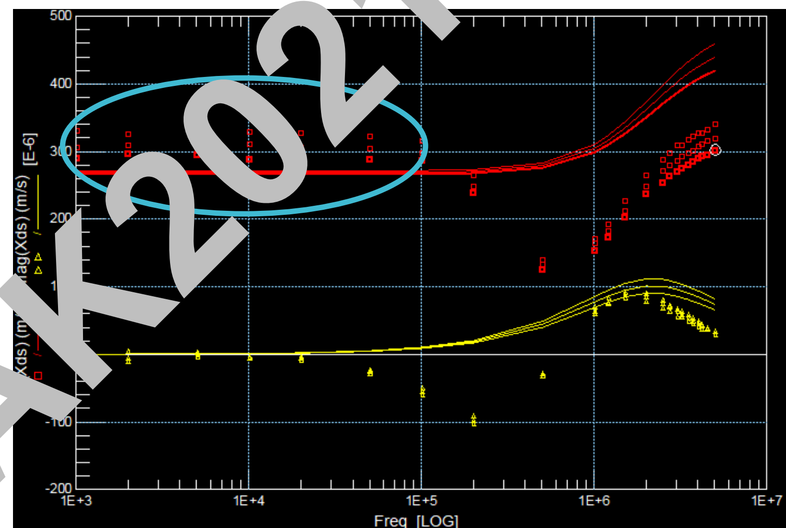
Radio Frequency

SHE is suppressed at high frequency

Abnormal kink at low frequency is observed in some devices

1. Inverse temperature trend
2. Floating body effect

Gds method is noise sensitive.
Current behavior along with frequency trend can be characterized.



Gds vs freq **@Transition Region**

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SHE Measurement Review

(Ⅰ) Pulse Method

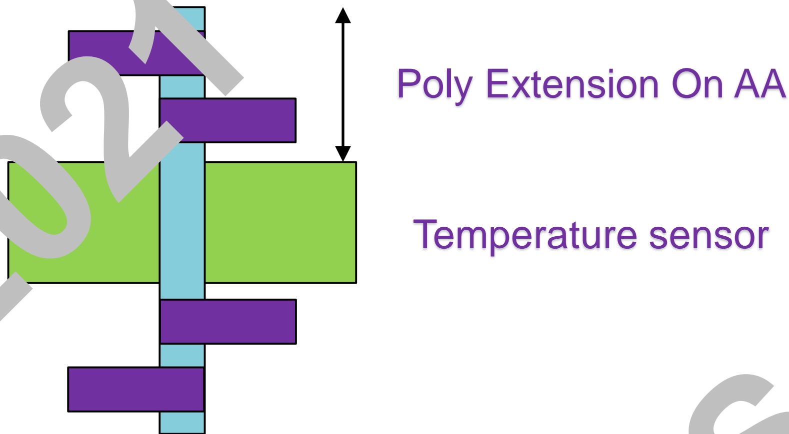
1. Complex Measurement & Extraction
2. Impedance Mismatch Problem
3. Expensive measurement instrument
4. SHE free data

(Ⅱ) Gds Method

1. Limited frequency range & precision
2. Noise sensitive
3. Complete Gth/Cth Extraction flow
4. Low cost

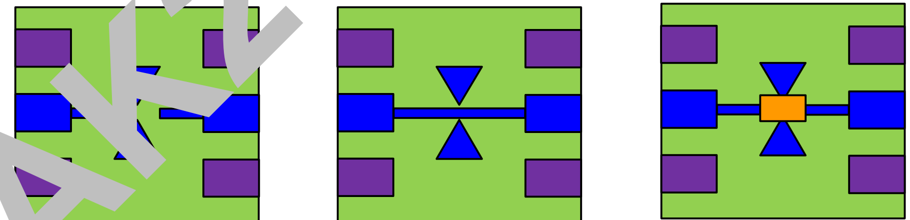
(Ⅲ) Gate Resistance Method

1. Special layout design
2. Low accuracy
3. Cth is unknown



(IV) RF Method

1. RF Layout & LF VNA
2. On wafer calibration & de-embedding
3. Wide frequency range
4. Consistent with RF data



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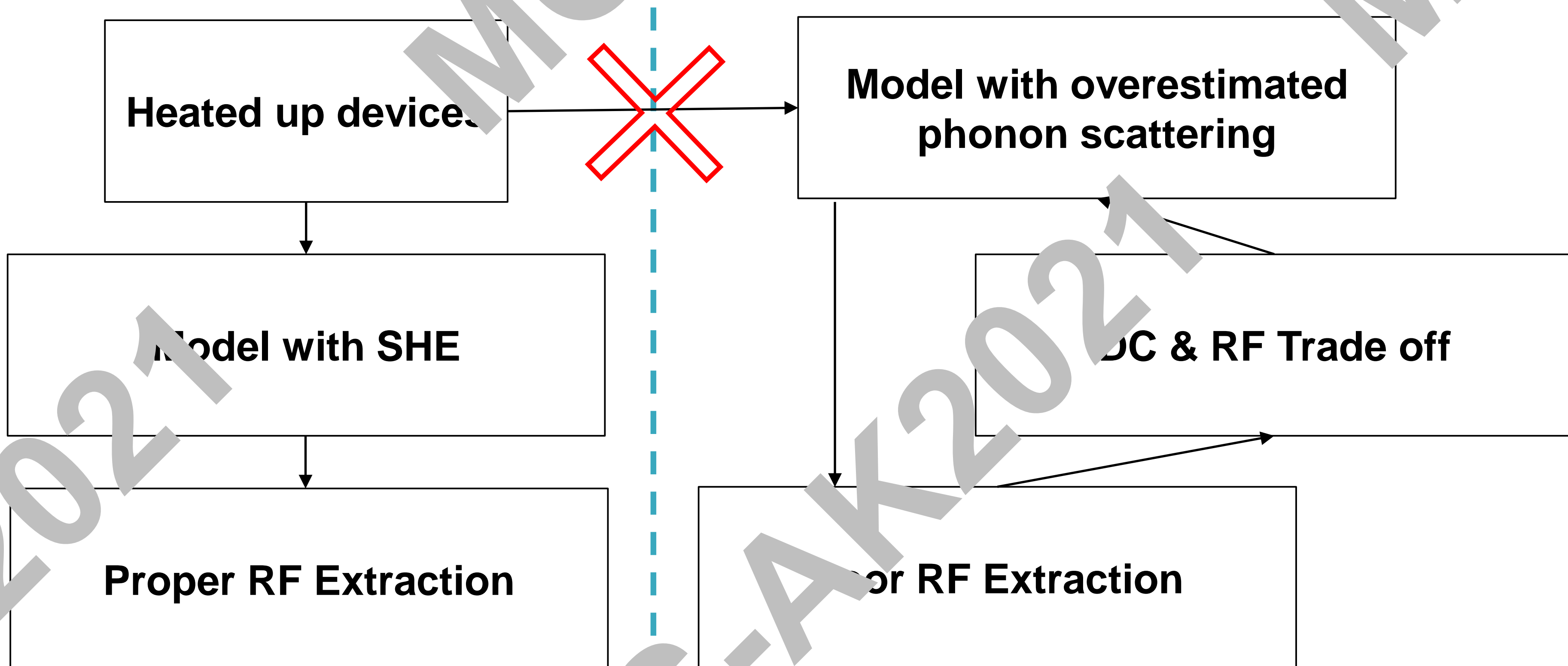
Why SHE is important?

- Phonon scattering may be overestimated
- Ring Oscillator QA failure
- Error increasing at high frequency
- RF extraction failure



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22nm FDSOI SPICE Model

- We have extracted a complete DC Device Model for 22nm FDSOI Technology.

Device	•MOS (Core/IO) , BJT, Resistor, Diode, Varactor
Level	•78 (BSIMIMG)
Effects	•Back Gate Bias, SHE, Gate-leakage, GIDL
Geometry	•Core: L[0.02~1um], W[0.08~3um] •IO: L[0.136~1.8um], W[0.16~22um]
Temp.	•-40~125°C
Voltage	•Gate: [-0.9~0.9V](core) / [-1.8~1.8V](IO) •BodyBias: [0-Vdd](NW)/[-Vdd-0](FW)
Corner	•TT, FF, SS, FS, SF

The contents of 22nm FDSOI model library

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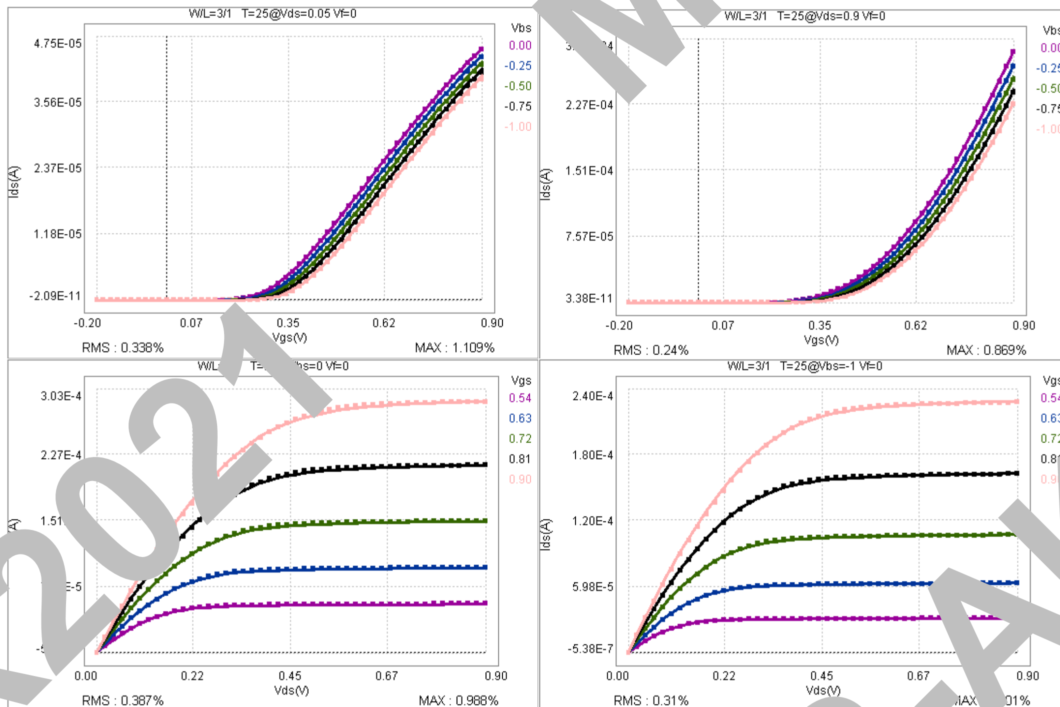
Model QA

Model Target：

Accuracy： **△Vtlin<5mV， △ Idsat<2%**

Physical： **Cover most physical effects（Bodybias/SHE）**

Scalable： **Model QA pass from Wmax/Lmax to Wmin/Lmin**



Device	ΔVtlin	ΔIdlin	ΔIdsat
Target	<5mV	<3%	<3%
NCore	<5mV	<1%	<1%
PCore	<5mV	<1%	<1%
NIO	<5mV	<2%	<2%
PIO	<5mV	<2%	<2%

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Model QA

Vthlin versus length at different temperature

vth_l_t(W=0.08@Vbs/Vds=0/-0.05)

-vth(V) vs l(um); t: -40.0000, 25.0000, 125.0000

RMS:0.621% MAX:1.659%

vth_l_t(W=0.24@Vbs/Vds=0/-0.05)

-vth(V) vs l(um); t: -40.0000, 25.0000, 125.0000

RMS:0.414% MAX:0.939%

vth_l_t(W=0.48@Vbs/Vds=0/-0.05)

-vth(V) vs l(um); t: -40.0000, 25.0000, 125.0000

RMS:0.447% MAX:1.093%

vth_l_t(W=3@Vbs/Vds=0/-0.05)

-vth(V) vs l(um); t: -40.0000, 25.0000, 125.0000

RMS:0.485% MAX:1.042%

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Model QA

Idsat versus length at different temperature

idsat_l_t(W=0.48@Vbs/Vgs/Vds=0/-0.9/-0.9)

-idsat(A): 2.45E-4, 1.86E-4, 1.26E-4, 6.70E-5, 7.53E-6

l(um): 0.02, 0.26, 0.51, 0.75, 1.00

RMS:0.548% MAX:1.241%

idsat_l_t(W=3@Vbs/Vgs/Vds=0/-0.9/-0.9)

t: -40.0000, 25.0000, 125.0000

-idsat(A): 1.58E-3, 1.20E-3, 8.16E-4, 4.31E-4, 4.71E-5

l(um): 0.02, 0.26, 0.51, 0.75, 1.00

RMS:0.452% MAX:1.560%

idsat_l_t(W=0.24@Vbs/Vgs/Vds=0/-0.9/-0.9)

t: -40.0000, 25.0000, 125.0000

-idsat(A): 1.19E-4, [illegible], [illegible], 3.28E-5, 3.92E-6

l(um): 0.02, 0.26, 0.51, 0.75, 1.00

RMS:0.661% MAX:[illegible]

idsat_l_t(W=0.08[illegible])

t: -40.0000, 25.0000, 125.0000

-idsat(A): 3.88E-5, 2.95E-5, 2.01E-5, 1.08E-5, [illegible]

l(um): 0.02, 0.26, 0.51, 0.75, 1.00

RMS:1.415% MAX:4.010%

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Ring Oscillator Results

- We have designed ring oscillator for the verification of FDSOI Model. As shown in the table, the simulation error is less than 10%.

Ring Oscillator	Invertor	F[illegible]	[illegible]	Simulation Delay	Test Delay	Accuracy
0.9V_Core	IN[illegible]	[illegible]	8	8.52	8.13	1.9%
	[illegible]	3	8	8.27	7.85	-0.8%
	NAND	1	8	13.07	12.46	4.5%
	NAND	3	8	24.91	24.37	2.1%
	NOR	1	8	13.52	13.5[illegible]	-[illegible]8%
	NOR	3	8	25.93	26.47	5.3%
1.8V_IO	INV	1	6	27.81	[illegible]6.8[illegible]	3.1%
	INV	3	6	53.66	52.07	2.8%
	NAND	1	6	40.[illegible]6	39.67	2.8%
	NAND	3	6	[illegible]6.01	85.73	-4.6%
	NOR	1	6	[illegible].08	50.59	-4.9%
	NOR	3	6	104.07	107.19	-4.1%

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Summary

- Measured data and simulation results show that FDSOI devices have more performance improvement than BULK process.
- Body biasing in FDSOI is an effective way to control device current.
- Self-heating effect in FDSOI is measured and verified by several methods.
- A high accuracy industry standard model for FDSOI MOSFETs using BSIM-IMG was successfully established.

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Thank you !

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