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Compact Transistor Model Parameter Extraction: Challenges and Directions

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Challenges in (Auto) Parameter Extraction

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Process Complexity

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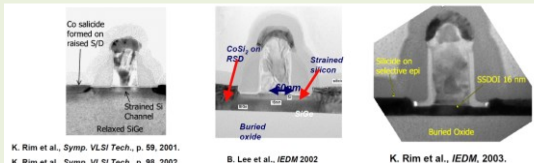
Planar Era | FinFET Era | Gate-All-Around Era

BSIM Models

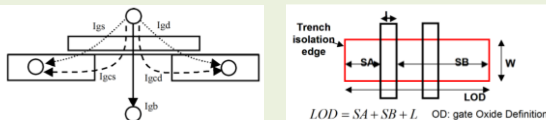
BSIM4 → **BSIM-BULK** → **BSIM-CMG (GEOMOD = 1)** → **BSIM-CMG (GEOMOD = 5)**

Foundry Process Evolution

- High-K/metal gate, strain Si



- GIDL, Ig, Iii, LDE (LOD, WPE, etc.)
- Self-heating, Monte-Carlo



2013-2014

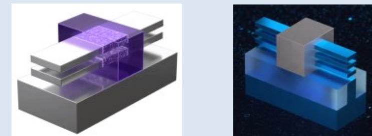
- Discrete NFIN instead of continuous W

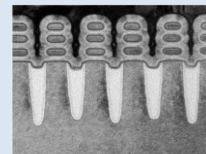
- Weak NFIN trend
- Optional EUVL
- More LDE, more self-heating in macro equations or TMI…

2020-2021

From 3 nm and below:

- EUVL a must-have
- Ferro-electric (NCFET)?
- Nanosheet, RibbonFET or MBCFET?





… 90 nm 65 nm 28 nm 16 nm … 7 nm 5 nm Moore's Law

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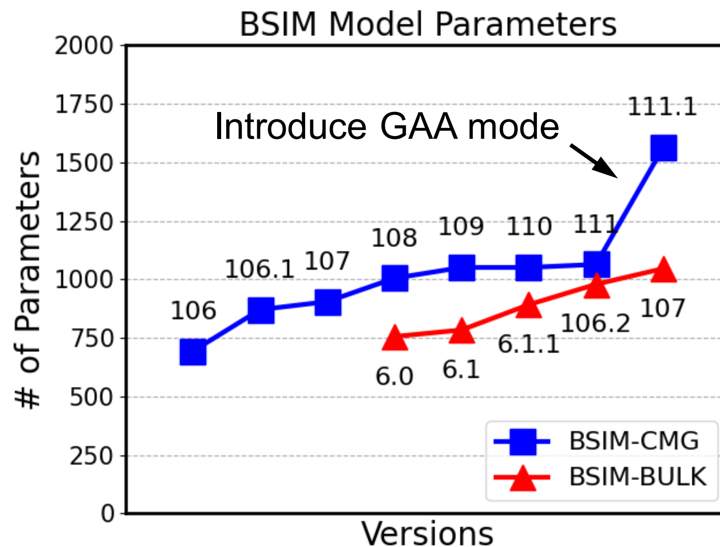
Model Complexity

- Recent iterations of BSIM models keep adding new physical and empirical parameters to account for new effects or to improve fitting quality.

- New BSIM-BULK and BSIM-CMG versions have over 1,000 parameters!
- This trend is unstoppable as technology nodes shrink and more small device effects appear.



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New Geometric Scaling

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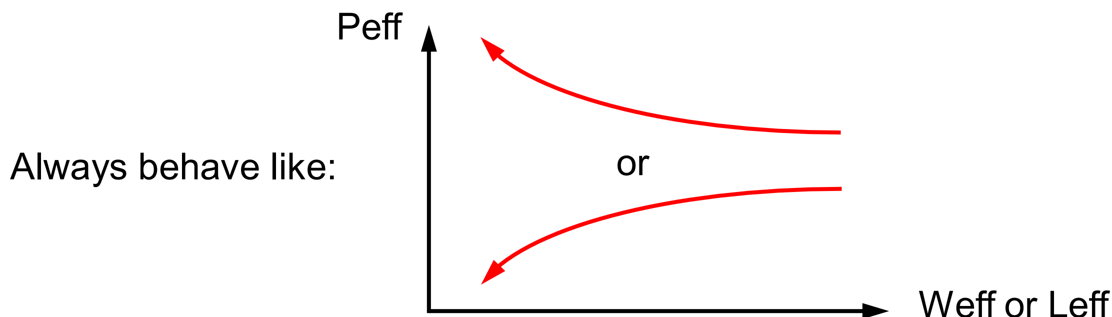
- In BSIM-BULK, new geometric scaling parameters such as (Pl, Pw, Plexp, Pwexp, etc.) further complicate the effective parameter (Peff) trend control.
- Example: In BSIM4, we only need to consider 4 geometric scaling parameters for channel doping (NDEP), and the W/L trend is well-behaved.

$$NDEP_{eff} = NDEP + \frac{LNDEP}{L_{eff}} + \frac{WNDEP}{W_{eff}} + \frac{PNDEP}{L_{eff} \times W_{eff}}$$

Always behave like:



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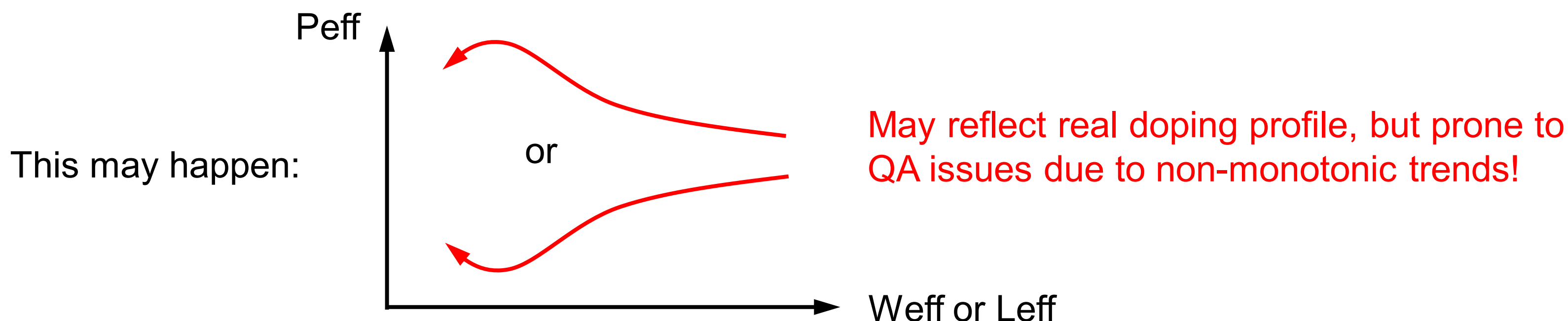
New Geometric Scaling

- In BSIM-BULK, eight more global scaling parameters were added including four power terms, which should be under tight control.

$$NDEP_{eff} = NDEP + \frac{LNDEP}{L_{eff}} + \frac{WNDEP}{W_{eff}} + \frac{PNDEP}{L_{eff} \times W_{eff}}$$

$$+ \frac{NDEPL1}{L_{eff}^{NDEPL1EXP}} + \frac{NDEPL2}{L_{eff}^{NDEPL2EXP}} + \frac{NDEPW}{W_{eff}^{NDEPWEXP}} + \frac{NDEPWL}{(L_{eff} \times W_{eff})^{NDEPWLEXP}}$$



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Control of Peff_total

- Control of total effective parameter (Peff_total), which is what BSIM uses to compute drain current, is a difficult task since there are many layers of contribution.
- In BSIM-CMG (GEOMOD=1):

Traditional geometric scaling

$$VSAT_{eff} = \left\{ \begin{array}{c} \left[VSAT + \frac{LVSAT}{L_{eff}} + \frac{NVSAT}{NFIN} + \frac{PVSAT}{L_{eff} \times NFIN} \right] \times \\ \left[1 + \frac{VSATN1}{NFIN} ln\left(\frac{NFIN}{VSATN2} \right) \right] + AVSAT \cdot exp\left(-\frac{L_{eff}}{BVSAT} \right) \end{array} \right\} \times [1 - AT \cdot (T - T_{nom})]$$

NFIN scaling

Length scaling

Temperature term

This goes into BSIM!

$$VSAT_{eff} = 0.5 \times VSAT_{eff} \cdot \left[1 + tanh\left(\frac{0.6 \cdot qV_{ds}}{kT} \right) \right] + 0.5 \times VSATR_{eff} \left[1 - tanh\left(\frac{0.6 \cdot qV_{ds}}{kT} \right) \right]$$

Forward mode

$if\ ASYMMOD = 1$

Reverse mode

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Peff_total Control

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- Even if you simplify your parameter settings to

$$VSAT_{eff} = \left[VSAT + \frac{LVSAT}{L_{eff}} + \frac{NVSAT}{NFIN} + \frac{PVSAT}{L_{eff} \times NFIN}\right] \times [1 - AT \cdot (T - T_{nom})]$$

$$where\ VSATN1 = AVSAT = ASYMMOD = 0$$

- It's easy to limit boundaries of separate parameters (e.g., VSAT and AT). But how to decide boundaries of geometric terms (LVSAT, NVSAT, PVSAT) since they are model scope dependent?
- How can you control total VSAT_eff, say, within (5000, 200000) given all pre-defined boundaries of LVSAT, NVSAT, PVSAT, and AT?
- Without relying on EDA tool, it's almost impossible for a human engineer to achieve this!

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Parameter Sensitivity

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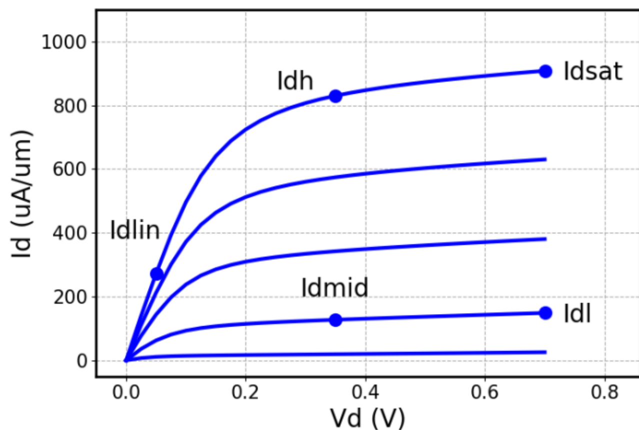
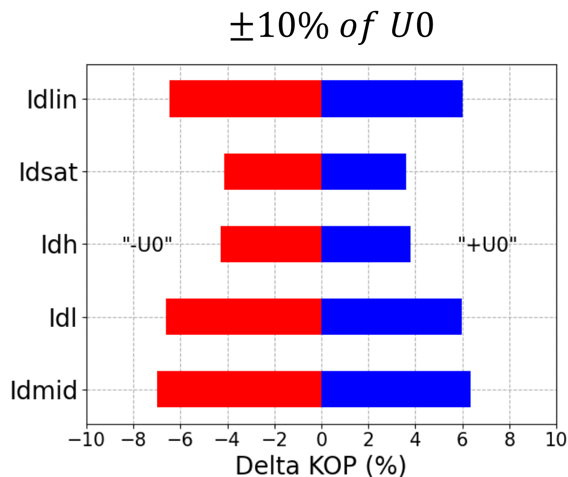
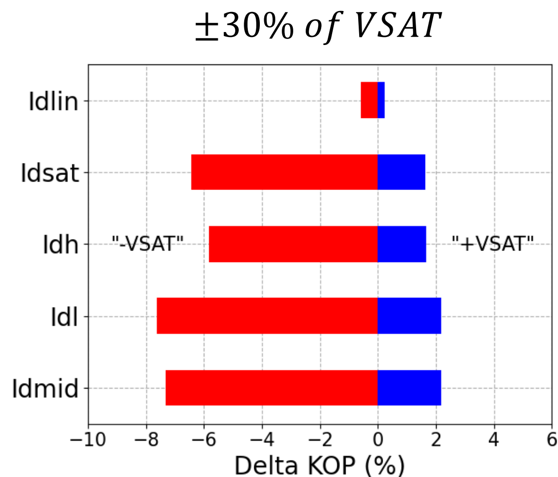
- The sensitivity of KOPs (key outputs) vs. parameters is not easy to understand without looking into BSIM equations.
- For example, while U0 has a more balanced sensitivity vs. KOPs, VSAT shows close-to-zero sensitivity for Idlin and asymmetric sensitivity for other saturation KOPs.







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Parameter Sensitivity

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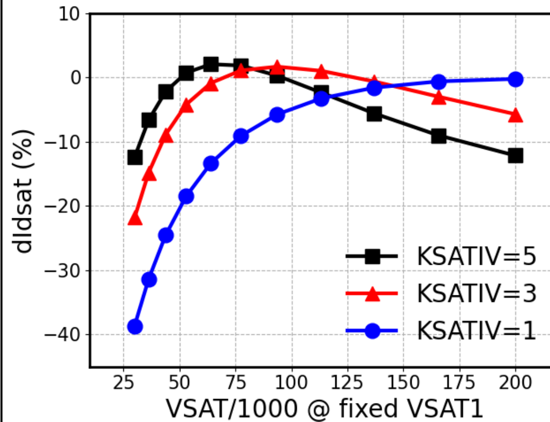
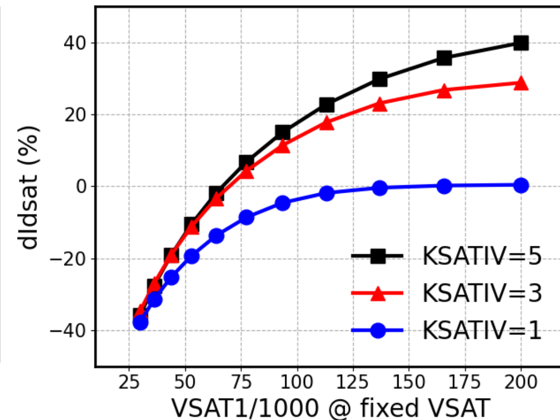
- Some equations are too complex to “understand” by looking at them.
- EDA tool needed to study their behavior in order to accumulate knowledge!

BSIM-CMG snippet of VSAT and KSATIV

```
Esat = 2.0 * VSAT_a / u0_a * Dmobs;
EsatL = Esat * Leff;
T6 = KSATIV_a * (qis + 2.0 * Vtm);
if (Rdss == 0.0) begin
    Vdsat = EsatL * T6 / (EsatL + T6);
end else begin
    WVCox = Weff0 * VSAT_a * cox;
    T0 = WVCox * Rdss;
    Ta = 2.0 * T0;
    Tb = T6 + EsatL + 3.0 * T6 * T0;
    Tc = T6 * (EsatL + 2.0 * T6 * T0);
    Vdsat = (Tb - sqrt(Tb * Tb - 2.0 * Ta * Tc)) / Ta;
end
Vdsat = `hypsmooth((Vdsat - 1.0e-3), 1.0e-5) + 1.0e-3;
T7 = pow((vds / Vdsat), MEXP_a);
T8 = pow((1.0 + T7), inv_MEXP);
Vdseff = min((vds / T8), vds);
```





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The Quick Answer…

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- To solve above issues, the quick answer is to use model extraction tools from EDA companies! Many have claimed they have **automatic extraction** capability.
- However, although many useful features are available, total Peff control and QA rule optimization are still very difficult jobs to do.
- What about data quality check and target trend check?
- How to teach a tool when “unphysical trend” happens and how to correct it?
- How to do simultaneous QA instead of post-QA?
- This is why majority of model extraction tasks are still done manually!

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Data Consistency Check

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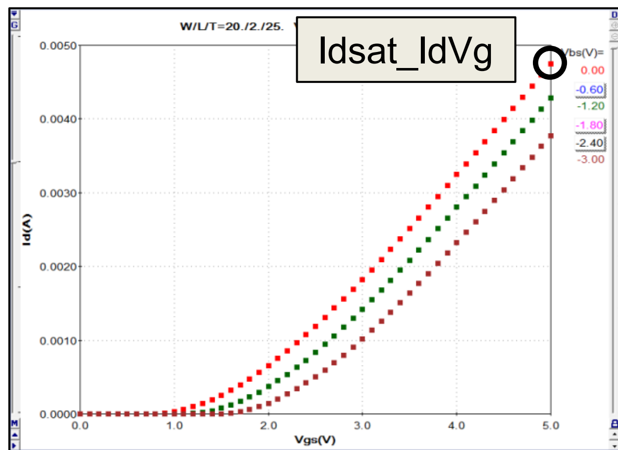
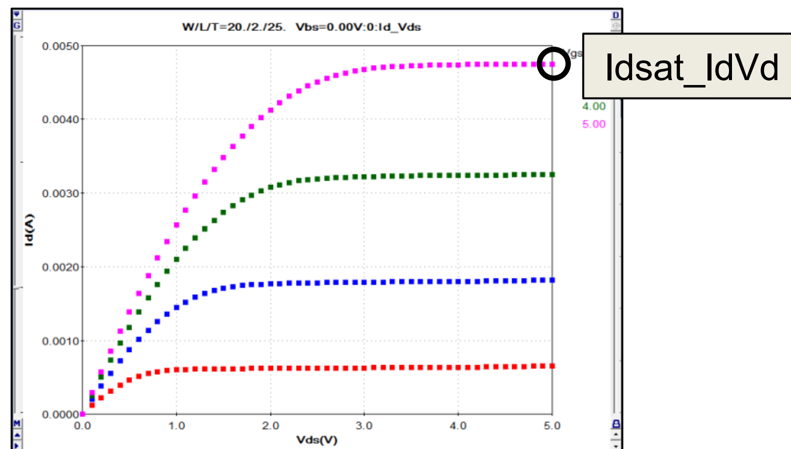
- It is acceptable for same-bias KOPs deviate 0.x% with each other due to measurement uncertainty.
- Example: if Idsat_IdVg is off Idsat_IdVd by, say, 3%, then there is reliability degradation for the data. Decision needs to be made as which curve to use or to re-measure.



vs.



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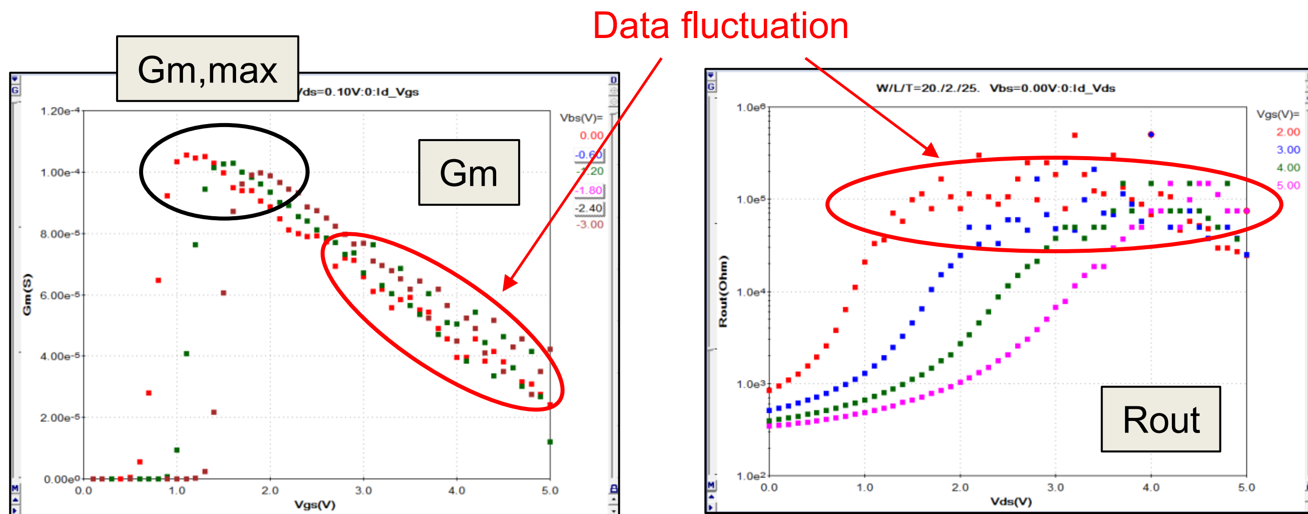
Gm/Rout Fluctuation

- Often Gm/Rout data shows fluctuation because they are derivatives. Can auto-extraction tools get reasonable fitting despite data fluctuation?
- Severe Gm,max fluctuation will impact Vtgm fitting error. Should focus on error of Id@Vtgm, not Vtgm itself!



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Spec-Driven Extraction Platform (SDEP) and DTCO Directions

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Bottleneck in DTCO

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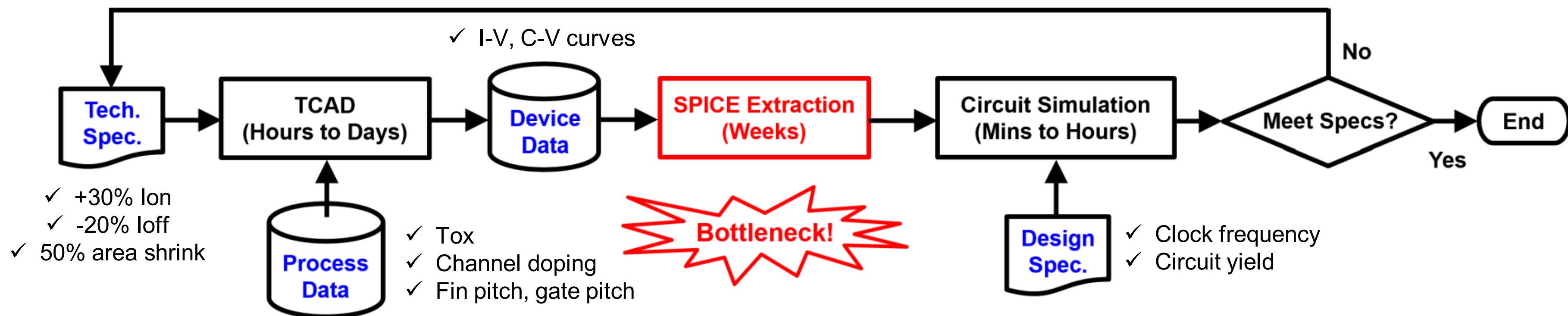
- Design-Technology Co-Optimization (DTCO) is required for foundries and IDMs to characterize PDK in a new process.
- Inefficient SPICE extraction is often the bottleneck of DTCO flow.
- SDEP to serve as SPICE extraction engine in a more efficient DTCO flow.



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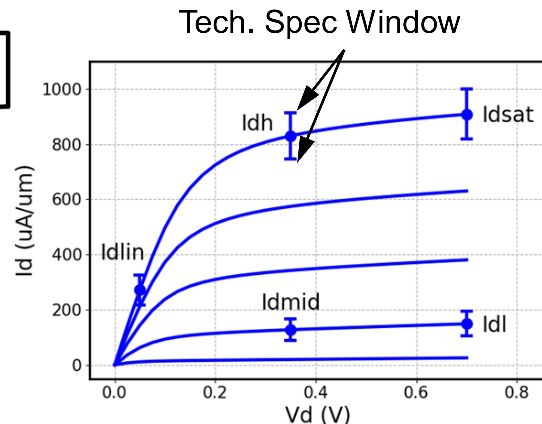
Technology Spec Window

Tech.
Spec.
TCAD
(Hours to Days)
Meet Specs?
No
Yes
Device
Data
Process
Data
"Technology Loop"
New
Tech. Spec.
Baseline Model
(Hours)
SDEP
Tech. Spec.
Window
No
Yes
End
Meet Specs?
Circuit Simulation
(Mins to Hours)
Retargeting
(Minutes)
Design
Spec.
SDEP
"Design Loop"

- Technology and design teams communicate through **technology spec. window.**

Tech. Spec Window



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Inside Technology Loop

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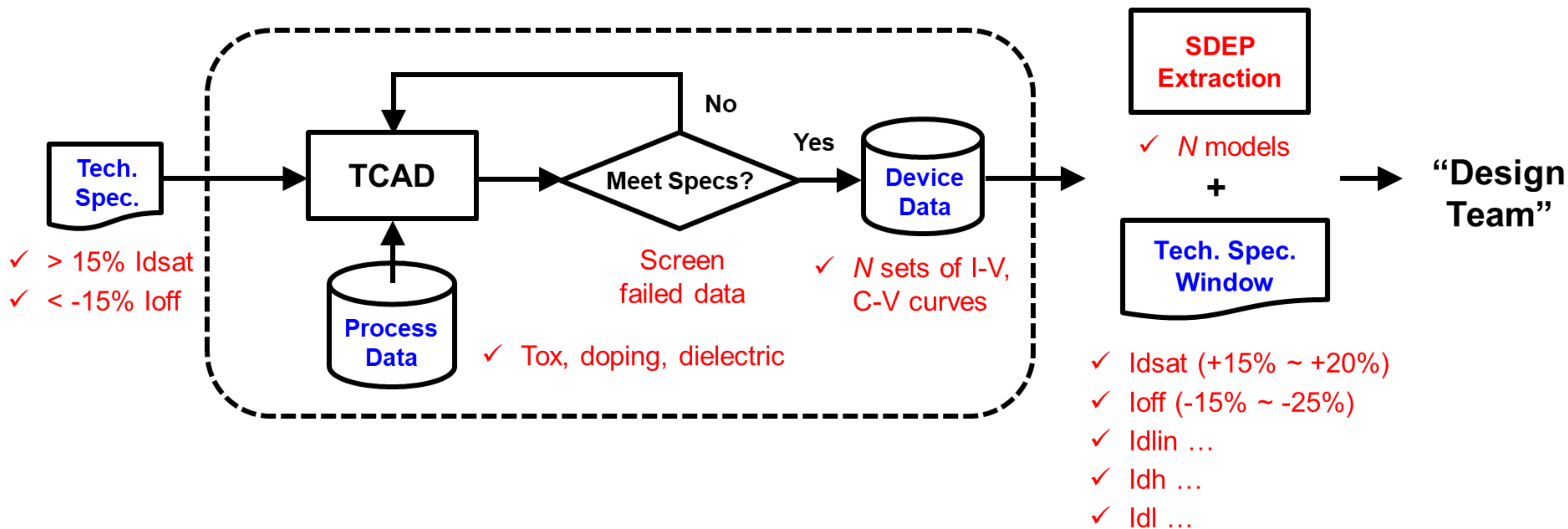

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Inside Design Loop

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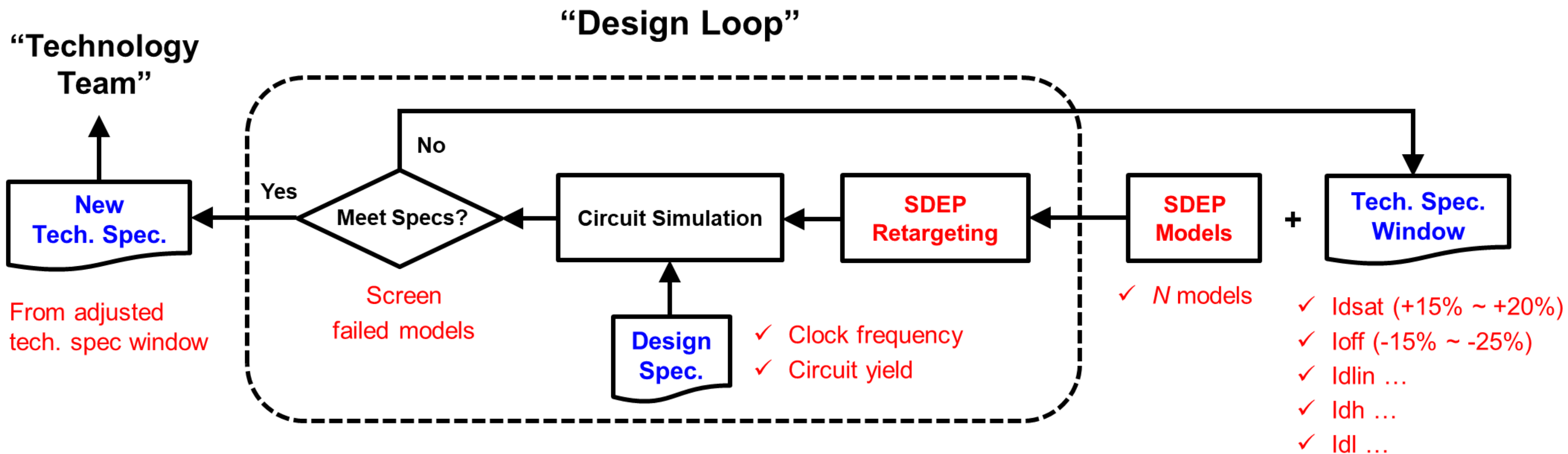

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Circuit–KOP Sensitivity

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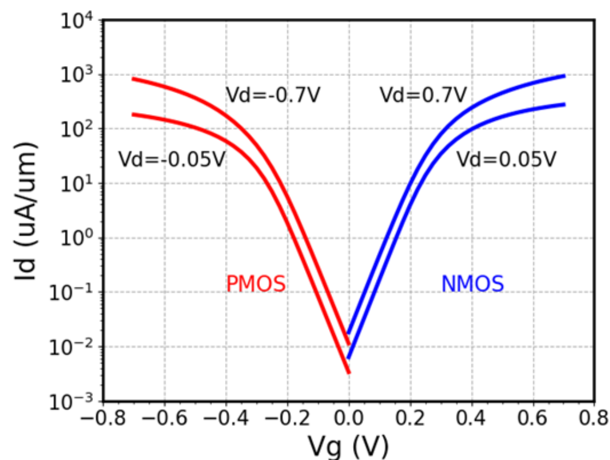
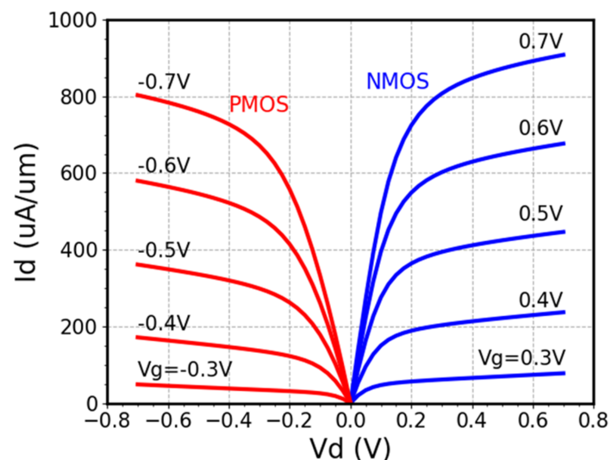
- Since SPICE generation is efficient, it is easier to study circuit KOPs vs. device KOPs using models **within technology spec. window**.
- A preliminary example is shown in our 2020 IEDM paper.





IRDS 5nm spec:

- ✓ Vdd = 0.7V
- ✓ Lg = 18nm
- ✓ Gate pitch = 48nm
- ✓ EOT = 1.1nm
- ✓ HFIN = 50 nm
- ✓ TFIN = 7 nm
- ✓ FPITCH = 28 nm

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Circuit–KOP Sensitivity

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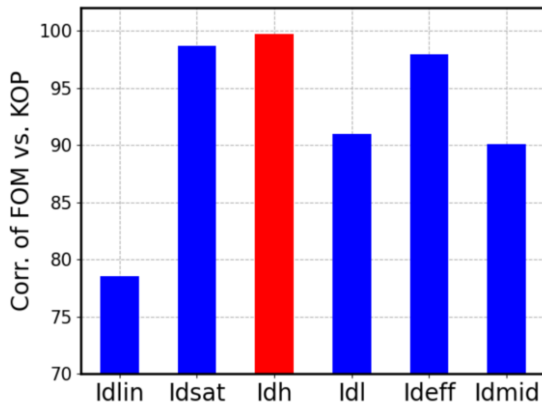
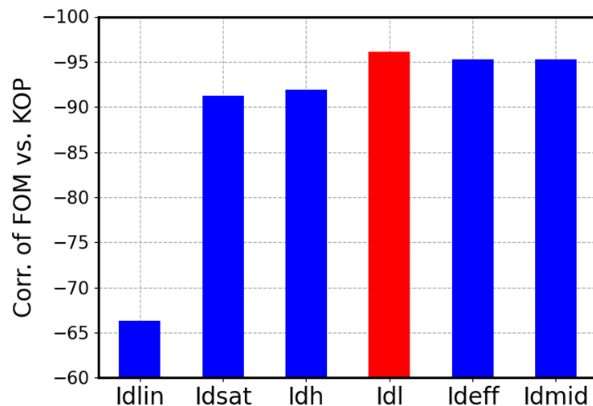
- With this analysis, designers can focus on key KOPs that affect circuits the most so they can better use the technology spec window with the technology team.

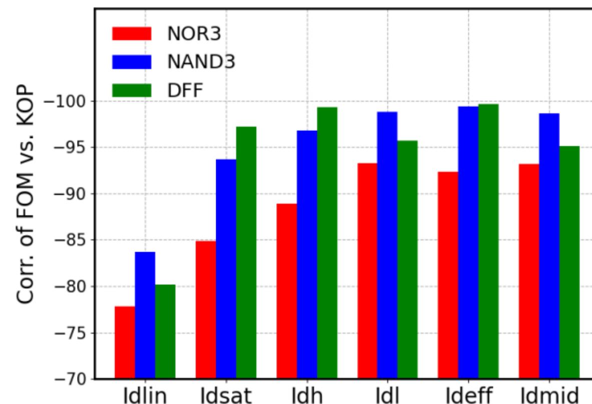
Oscillation frequency of a 3-stage ring oscillator (RO):



Read static noise margin (SNM) of a 6T SRAM:



Time delay of NOR3, NAND3, DFF gates:



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Summary

- We pointed out major challenges in today's model extraction, both in manual tuning and auto-extraction.
- SDEP is Primarius's technology breakthrough to counter these challenges.
- SDEP can play a more important role in a newly structured DTCO flow.
- Technology spec window greatly links the technology and design teams, creating a more operable working model for each team.
- Designers can focus on key KOPs through circuit-KOP sensitivity.

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- Our IEDM DTCO paper: https://ieeexplore.ieee.org/document/9372118

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